TEA5766UK

Stereo FM radio + RDS

Rev. 01 — 22 March 2007 Product data sheet

1. General description

The TEA5766UK is a single chip electronically tuned FM stereo radio with Radio Data System (RDS) and Radio Broadcast Data System (RBDS) demodulator and RDS/RBDS decoder, for portable application with fully integrated Intermediate Frequency (IF) selectivity and FM demodulation.

The radio is completely adjustment free and only requires a minimum of small and low cost external components.

The radio can tune to the European, US and Japanese FM bands. It has a low power consumption at a low supply voltage.

The TEA5766UK application software is compatible to the TEA5764 software to enable easy design-in for customers.

2. Features

- High sensitivity due to integrated low noise Radio Frequency (RF) input amplifier
- FM mixer for conversion of the US/Europe (87.5 MHz to 108 MHz) and Japanese FM band (76 MHz to 90 MHz) to IF
- Preset tuning to receive Japanese TV audio up to 108 MHz
- Autonomous search tuning, 100 kHz grid
- RF automatic gain control circuit
- LC tuner oscillator operating with integrated varicaps and one low-cost chip inductor
- Fully integrated FM IF selectivity
- Fully integrated FM demodulator
- 32768 Hz external reference frequency
- Phase Locked Loop (PLL) synthesizer tuning system
- IF counter, 7-bit output via control interface
- Level detector, 4-bit level information output via the control interface
- Soft mute, signal depending mute function, can be switched on or off via the control interface
- Mono/stereo blend, signal depending gradual change from mono to stereo, can be switched on or off via the control interface
- Standby mode
- Software programmable port
- Fully integrated RDS/RBDS demodulator in accordance with EN 62106
- RDS/RBDS decoder with memory for two RDS data blocks provides block synchronization and error correction; block data and status information are available via the I^2C-bus

- Interrupt flag
- Interrupt line

3. Quick reference data

Table 1. Quick reference data

Under all conditions a reference clock of 32.768 kHz is present.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
General electrical parameters							
V_{CCA}	analog supply voltage			2.6	2.7	3.6	V
$V_{CC(VCO)}$	VCO supply voltage			2.6	2.7	3.6	V
I_{CCA}	analog supply current	operating	[1]	-	13.5	17	mA
		Standby mode	[1]	-	-	5	µA
V_{CCD}	digital supply voltage			2.6	2.7	3.6	V
I_{CCD}	digital supply current	operating; RDS off		-	350	450	µA
		operating; RDS on		-	0.75	1.5	mA
		Standby mode		-	5	10	µA
		Sleep mode; only in I^2C-bus; BUSEN = HIGH		-	16	25	µA
$V_{VREFDIG}$	voltage on pin VREFDIG	$V_{VREFDIG} \leq V_{CCD}$		1.65	1.8	V_{CCD}	V
$I_{VREFDIG}$	current on pin VREFDIG			0	0.5	1	µA
		Standby mode		0	0.5	1	µA
General operating conditions							
$f_{i(FM)}$	FM input frequency			76	-	108	MHz
T_{amb}	ambient temperature	device meets all specifications		–20	-	+85	°C
		TEA5766UK functional, specification not guaranteed		–30	-	+85	°C

[1] Includes both analog supply current on pin V_{CCA} and VCO supply current on pin $V_{CC(VCO)}$.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TEA5766UK	WLCSP25	wafer level chip-size package; 25 bumps; 3.3 × 3.25 × 0.6 mm	TEA5766

5. Block diagram

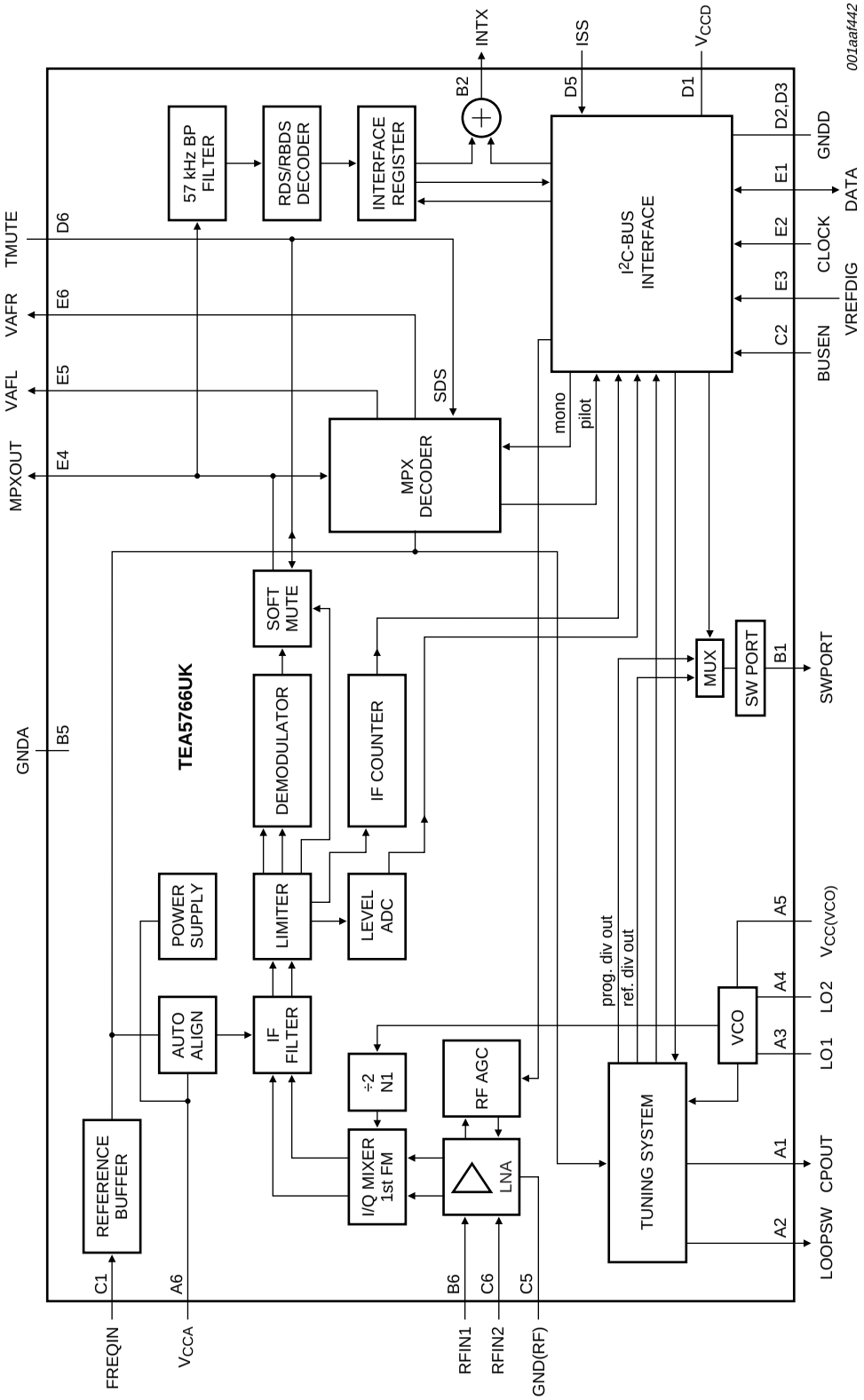


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

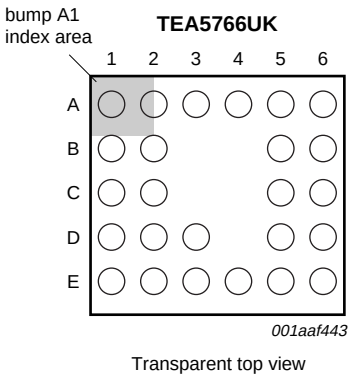


Fig 2. Ball configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
CPOUT	A1	charge pump output of synthesizer PLL
LOOPSW	A2	switch output of synthesizer PLL loop filter
LO1	A3	local oscillator coil connection
LO2	A4	local oscillator coil connection
$V_{CC(VCO)}$	A5	Voltage Controlled Oscillator (VCO) supply voltage
V_{CCA}	A6	analog supply voltage
SWPORT	B1	software programmable port output
INTX	B2	interrupt output
GNDA	B5	analog ground
RFIN1	B6	RF input 1
FREQIN	C1	input for 32.768 kHz reference frequency
BUSEN	C2	• I^2C-bus enable input • SPI-bus chip select input
GND(RF)	C5	RF ground
RFIN2	C6	RF input 2
V_{CCD}	D1	digital supply voltage
GNDD	D2	digital ground
GNDD	D3	digital ground
ISS	D5	I^2C-bus or SPI-bus selection input[1]
TMUTE	D6	time constant capacitor connection for soft mute
DATA	E1	input/output and control interface data line
CLOCK	E2	control interface clock line input
VREFDIG	E3	digital reference voltage for control interface

Table 3. Pin description *...continued*

Symbol	Pin	Description
MPXOUT	E4	multiplex signal (MPX) output
VAFL	E5	left audio output
VAFR	E6	right audio output

[1] The ISS pin the bus type can be selected, see Section 10.1.

7. Functional description

7.1 Low noise RF amplifier

The Low Noise Amplifier (LNA) input impedance together with the LC RF input circuit defines an FM band filter. The gain of the LNA is controlled by the RF Automatic Gain Control (AGC) circuit to prevent overdrive of the subsequent circuits.

7.2 FM mixer

The FM quadrature mixer converts the received RF (76 MHz to 108 MHz) to the IF of 225 kHz. Downconversion is achieved by multiplication of the RF with the Local Oscillator (LO) frequency. Image frequency suppression is achieved by using quadrature signal processing.

7.3 VCO

The LC tuned VCO provides the local oscillator signal for the downconversion of the RF signal to IF. The VCO is tuned to the double frequency required for the downconversion. The LO is divided by two to provide the quadrature oscillator signals for the downconversion process. The VCO frequency range is from 150 MHz to 217 MHz. Integrated varactors are used for the VCO tuning. The only external component used for the VCO is a coil.

7.4 Reference frequency

An external 32.768 kHz reference frequency is used as system clock. The reference clock specifications are given in Section 13.2.

The reference frequency is used for:

- Synthesizer PLL reference frequency
- Timing for the IF counter
- Adjustment of the 38 kHz VCO for the stereo decoder
- Auto alignment of the selectivity as well as the demodulator filters
- Auto alignment of the 57 kHz RDS filter

7.5 Tuning system

The PLL synthesizer tuning system is suitable to operate with a 32.768 kHz reference frequency. A 14-bit word is used to tune the radio, see Table 15. Calculation of this 14-bit word shall be done as follows:

Formula for high-side injection:

$$N_{DEC} = \frac{4 \times (f_{RF} + f_{IF})}{f_{ref}} \quad (1)$$

Formula for low-side injection:

$$N_{DEC} = \frac{4 \times (f_{RF} - f_{IF})}{f_{ref}} \quad (2)$$

where:

N_{DEC} = decimal value of PLL word

f_{RF} = wanted tuning frequency (Hz)

f_{IF} = intermediate frequency of 225 kHz

f_{ref} = reference frequency of 32.768 kHz

Example for receiving a channel at 100.1 MHz:

$$N_{DEC} = \frac{4 \times (100.1 \times 10^6 + 225 \times 10^3)}{32768} = 12246.704 \quad (3)$$

Value 12246.704, is rounded down to the lowest integer value, being 12246, the PLL word becomes 2FD6h.

The result found using Equation 1 or Equation 2 must always be rounded to the lowest integer value (truncation). Via the control interface this value can be written to register FRQSET and the TEA5766UK will then start an autonomous search beginning at this frequency or go to a preset channel at this frequency. When the application is built according to the application diagram of Figure 21 and with the preferred components, the tuning system will settle to the new frequency within 40 ms.

The PLL is triggered by writing one of the four bytes of the FRQSET and TNCTRL and registers.

The Lock Detect (LD) bit in register TUNCHK will be set after PLL lock detection (see Table 18).

7.6 Band limits

The TEA5766UK can be switched to the Japanese FM band or the US/Europe FM band. Bit BLIM in register TNCTRL (see Table 16) set to logic 0 enables the US/European band (87.5 MHz to 108 MHz) and BLIM set to logic 1 enables the Japanese band (76 MHz to 90 MHz).

7.7 RF AGC

The RF AGC (or wideband AGC) prevents overloading and limits the amount of intermodulation products created by strong adjacent channels. Default the RF AGC is on and it can be turned off via the control interface.

The TEA5766UK also has an in-band AGC to prevent overloading by the wanted channel itself. The in-band AGC is always on.

7.8 IF filter

Fully integrated IF filter with a center frequency of 225 kHz.

7.9 FM demodulator

Fully integrated FM quadrature demodulator.

7.10 IF counter

7.10.1 IF counter correct channel checking

The received RF signal is converted down to a 225 kHz Intermediate Frequency (IF). The IF is measured by means of a frequency counter. A correct IF frequency measurement result indicates that the radio is tuned to a valid channel and not to an image or a channel with high interference. The 7-bit IF counter output can be read via the control interface. The IF counter is continuously active and can be read at any time via the bus. It also activates a flag when the IF count result is outside the IF count valid result window; see also Section 8.2.4.

7.10.2 IF counter count time

Before a tuning cycle is initiated the IF count period can be set to 2 ms or to 15.6 ms with bit IFCTC in register TNCTRL (see Table 16). When the IF count period is set to 2 ms, initiating the tuning algorithm with a preset (SM = 0) will always give an RDS update as shown in Section 7.21. In case the IF count time is set to 15.6 ms the tuning flowchart of Section 7.20 is used. Once tuned, the IF count period is always 15.6 ms.

7.11 Level voltage generator and level analog-to-digital converter

The level voltage reflects the received field strength at the antenna. The analog level voltage is digitized to 4 bits by the level Analog-to-Digital Converter (ADC). This level ADC is continuously active and the output can be read at any time via the control interface. The level ADC information is used during search as well as preset tuning to compare the received signal strength with a search stop level (see Section 8.2.5). A flag will be set to indicate that the level voltage is reduced below a programmable threshold value (see Section 8.2.5). The threshold value is relative to the search stop level. The hysteresis between the search stop level and the threshold level can be selected by bit LHSW (see Table 19, Table 20 and Section 8.2.5).

When the ADC level is set to its minimum value 3, the search algorithm will only stop at channels having an RF level higher than or equal to ADC level 3. After completing the search algorithm and being tuned to a station, due to the hysteresis the effective limit will be set to 0. This means that the continuous ADC level check will never set the LEVFLAG.

7.12 Mute

7.12.1 Soft mute

The low-pass filtered level voltage drives the softened attenuator. At low RF input levels, the audio output is faded and hence also the noise. The softened function can be turned on/off via the control interface, bit SMUTE in register TNCTRL (see Table 16).

7.12.2 Hard mute

With the MU bit of the TNCTRL register byte 2 (see Table 16), the audio outputs VAFL and VAFR can be hard-muted; this means they are put in high-impedance state. The same can be done by setting the bits Left Hard Mute (LHM) or Right Hard Mute (RHM) in register TESTREG (see Table 19), which mute only one output at a time (or both when both set). When one output is muted the stereo decoder switches to mono. When he TEA5766UK is in Standby mode the audio outputs are in high-impedance state (see Table 4).

7.12.3 Audio Frequency Mute (AFM)

With the AFM bit of the TNCTRL register byte 1, the audio signal can be muted. The audio pins maintain their functional impedance and DC-biasing level while the audio signal is muted. The audio frequency mute is automatically activated during preset as well as search tuning modes as shown in the flowchart of Figure 4. The audio frequency mute can be disabled in software test mode when bit TM = 1 and bit AFMDIS = 1.

7.12.4 Specification of mute modes

Table 4. Specification of mute modes

Type	Description	VAFL		VAFR	
		Impedance	Mode	Impedance	Mode
AFM	audio frequency mute	350 Ω	muted	350 Ω	muted
RHM	right hard mute	350 Ω	mono audio	> 500 kΩ	muted
LHM	left hard mute	> 500 kΩ	muted	350 Ω	mono audio
MU	hard mute	> 500 kΩ	muted	> 500 kΩ	muted
Standby	standby	> 1 MΩ	-	> 1 MΩ	-
SMUTE	soft mute	RF sensitive audio level; has no influence on mute pin or impedance			

7.13 MPX decoder

The stereo decoder PLL is adjustment free. The stereo decoder can be switched to mono via the control interface.

7.14 Signal depending mono/stereo blend (stereo noise cancellation)

With decreasing RF input level the MPX decoder blends from stereo to mono to limit the output noise. The continuous mono-to-stereo blend can also be programmed via the control interface to an RF level depending switched mono to stereo transition. Stereo noise cancellation can be switched on or off via the control interface using bit SNC in register TNCTRL (see Table 16). When stereo noise cancellation is switched off, the radio switches from mono to stereo instead of blending. The RF input voltage where blending starts can be switched with bit SNCLEV in register TESTREG (see Table 19).

7.15 Software programmable port

One software programmable port SWPORT (CMOS output) is available and can be controlled via the control interface. With bit SWPM = 1 the software port (pin SWPORT) functions as the output for the FRRFLAG and with bit SWPM = 0 the software port output follows bit SWP. Bits SWP and SWPM are in register TNCTRL (seeTable 16). In software

test mode the software port outputs signals according to Table 21. Software test mode is selected by setting bit TM of register TESTREG (see Table 19). The software port is not disabled by the PUPD bits (see Section 7.16).

7.16 Standby mode

With the PUPD[1:0] (power-up/power-down) bits the radio can be put in Standby mode. Standby mode is defined as where the TEA5766UK has all supply voltages available but the circuits are powered down via software (PUPD) or after power-on reset. The RDS part can be turned off separately, using one of the PUPD bits. After a power-on reset or when the TEA5766UK is in Standby mode, the TEA5766UK is still accessible via the control interface, but takes only a limited amount of power from the supply. The software programmable port maintains active to allow peripheral devices to be controlled. The audio outputs are hard-muted.

In I^2C-bus mode when pin BUSEN = HIGH and the circuits are powered down via software (PUPD) the TEA5766UK is in Sleep mode. In this Sleep mode the TEA5766UK is accessible via the bus, but the radio part is not active. The $I_{VREFDIG}$ current is higher than in Standby mode.

When the supply voltages V_{CCA} and V_{CCD} are made 0 V and pin VREFDIG = HIGH, all I/Os, the audio outputs and the reference clock input are in high-impedance state. The power supplies can be switched on in any order.

7.17 Power-on reset

After start-up of V_{CCA} and V_{CCD}, a power-on reset circuit will generate a reset pulse and the registers will be set to their default values as shown in Table 12. The power-on reset is effectively generated by V_{CCD}. Power-on reset: the audio output pins are in high-impedance state (hard mute) and all other bits are set default according to the tables in Section 11. To initialize the TEA5766UK all bytes have to be transferred.

7.18 RDS/RBDS demodulator

Fully integrated RDS/RBDS demodulator, uses the reference frequency (32678 Hz) of the PLL synthesizer tuning system. The RDS demodulator recovers and regenerates the continuously transmitted RDS or RBDS data stream of the multiplex signal (MPXRDS) and provides the signals clock (RDCL), data (RDDA) for further processing by the integrated RDS decoder.

7.19 RDS/RBDS decoder

The RDS decoder provides block synchronization, error correction and flywheel function for reliable extraction of RDS or RBDS block data. Different modes of operation can be selected to fit different application requirements. Availability of new data is signalled by bit DAVFLG and output pin INTX, which generates an interrupt. Up to two blocks of data and status information are available via the I^2C-bus in a single transmission.

The behavior of the DAVFLG is described in Section 9.

7.20 Auto search and preset mode

In search mode TEA5766UK can search channels automatically.

When the INTX signal is used as an interrupt to the host processor to indicate a search stop, the INTMSK register must be reset and only bit FRRMSK must be set. In this way the host processor will only be interrupted when the search/preset algorithm is ready. Search mode is initiated setting the SM bit to logic 1 in the FRQSET register. When bit SUD is logic 0 then it searches down and when SUD is logic 1 it searches up. The tuner starts searching at the frequency where it is or at a new start frequency programmed to the tuner. With the Search Stop Level (SSL[1:0]) bits the minimum field strength of channels to be found can be set. The tuner will stop on a channel with a field strength equal to or higher than this reference level and then will check the IF frequency. When both are valid the search mode stops. If the level check or the IF count fails, it continues the search. When no channels are found the TEA5766UK stops searching when it has reached the band-limit and bit BLFLAG goes to logic 1. A search always stops with bit FRRFLAG being set and a hardware interrupt. Figure 4 shows this procedure.

After this interrupt the TEA5766UK will keep its status and will not update the INTREG, FRQCHK and TUNCHK tuner registers for a period of 15.6 ms. The state of the TEA5766UK can be checked by reading tuning registers: INTREG, FRQCHK and TUNCHK. Table 5 shows the possible states after an auto search or a preset.

A preset is done by setting bit SM to logic 0 and writing a frequency to byte FRQSETMSB. The tuner jumps to the selected frequency and sets bit FRRFLAG when it is ready. After this interrupt the TEA5766UK will keep not update the tuner registers for a period of 15.6 ms. The state of the TEA5766UK can be checked by reading registers: INTFLAG, FRQCHK and TNCTRL. Table 5 shows the possible states after an auto search or preset.

Table 5. Tuner truth table[1]

Bit			Comment
IFFLAG	BLFLAG	FRRFLAG	
0	0	0	this cannot occur if INTX has gone LOW and only IFMSK, FRRMSK and BLMSK were set
0	0	1	channel found during search/preset FRRMSK set
0	1	0	not a valid state
0	1	1	a valid channel found and the band limit has been reached during a search; BLMSK or FRRMSK set
1	0	0	not a valid state

Table 5. Tuner truth table[1] *…continued*

Bit			Comment
IFFLAG	BLFLAG	FRRFLAG	
1	0	1	a preset or search has been done, but the wanted channel has a valid RSSI level but fails the IF count; when AHLSI was set HLSI must be toggled and a new PLL value must be programmed; FRRMSK set
1	1	0	not a valid state
1	1	1	band limit is reached during search; no valid channel found; BLMSK or FRRMSK set

[1] This table is valid until 31.25 ms after the tuning cycle has completed. It shows the outcome of the flag register when a read is done after INTX has gone LOW with the condition that no other mask bits are set than shown in the table.

7.20.1 Auto high-side and low-side injection stop switch

The channel quality can sometimes be improved in case of image frequency interference. This can be achieved if the Local Oscillator (LO) injection is positioned at the opposite side of the wanted channel (see Figure 3). Indication for image frequency interference can be derived from the IF frequency counter. To enable this feature the AHLSI bit must be set to logic 1.

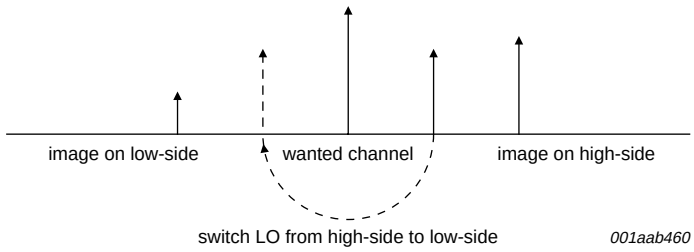


Fig 3. Switch LO from high-side injection to low-side injection using the HLSI bit

The search/preset algorithm will stop and generate an interrupt event after the detection of a valid RSSI level in combination with a frequency outside the IF frequency window. The host processor can detect this state by reading the interrupt register. Swap of the LO injection is achieved by inversion of bit HLSI in combination with a new tuning word for the changed oscillator frequency (see Section 7.5).

7.20.2 Muting during search or preset

During preset and search the tuner is always muted, which is done by the algorithm itself. When the AHLSI bit is set and the tuner has stopped during a preset or a search because of a wrong IF count, the tuner keeps muted and generates an interrupt event. In this way the host processor can switch the high or low setting quietly and waits for the new result.

All these mute actions are done by blocking the audio signal and the audio output will keep its DC level and stay in low-impedance state i.e. 50 Ω (see Table 4). A hard mute with the MU bit will cause a plop.

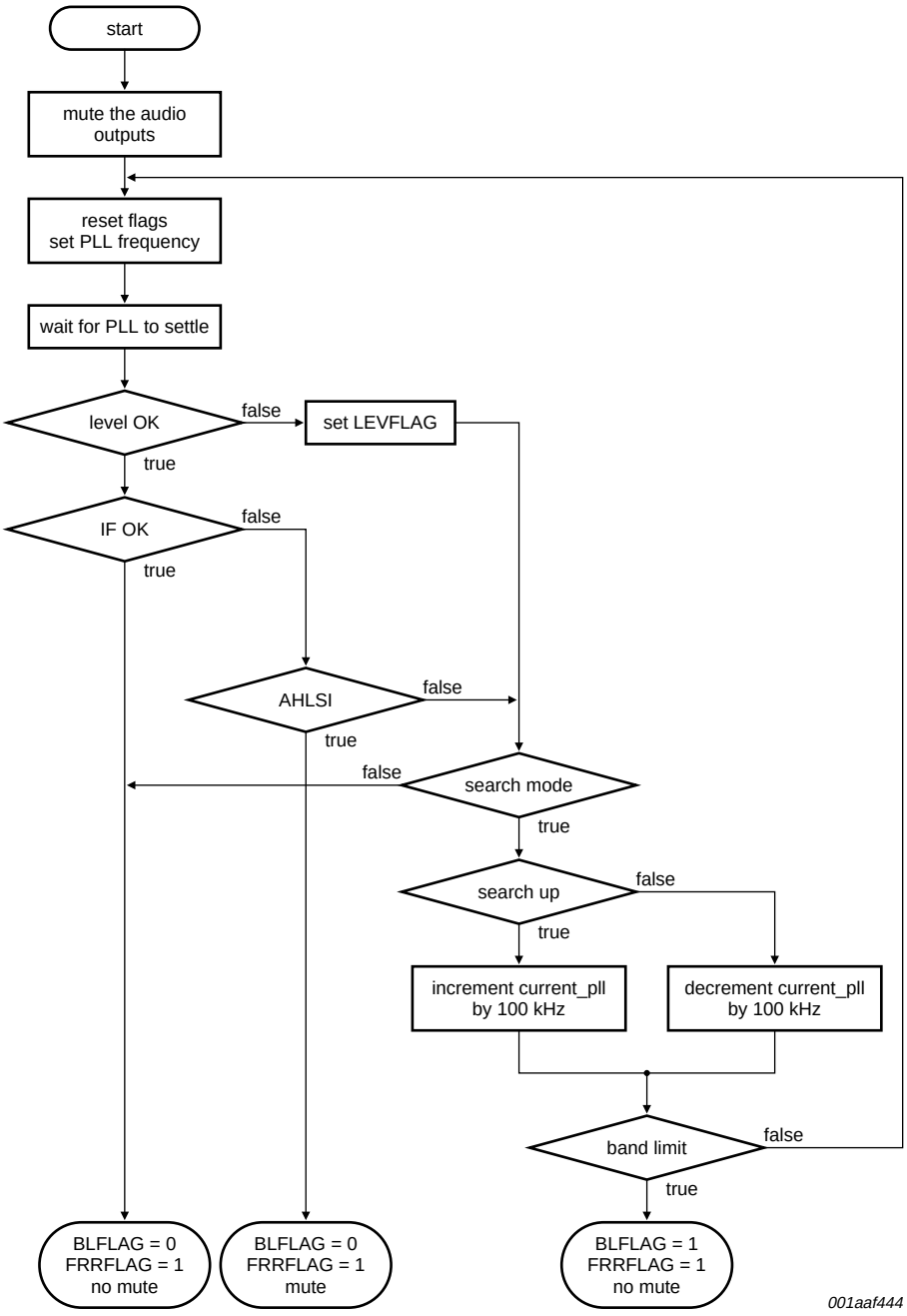


Fig 4. Flowchart auto search or preset

7.21 RDS update or alternative frequency jump

A channel which transmits RDS data can have alternative channels which carry the same information. These alternative channel frequencies are in the RDS data, so the host processor can read the alternative frequencies and store them in a memory. More details on this subject can be found in section 3.5 of *RDS: The Radio Data System, Dietmar Kopitz and Bev Marks*.

The tuner can do an RDS update. This is a preset, but with a 2 ms IF count time. The tuner will jump to the alternative frequency and check the level and the IF count using a 2 ms count time. When RSSI level check is above the specified level and the IF count result is within the limits then the tuner will stay at the alternative frequency and stay muted. The host processor can now decide what to do. If the alternative frequency is not valid it will jump back to the frequency it came from. The algorithm will finish with the FRRFLAG being set and generate an interrupt. After this interrupt the TEA5766UK will not measure the IF count for a period of 15.6 ms. 15.6 ms after completing an RDS jump a measurement of the IF count will start and hence the IF count result and the IFFLAG will be updated 31.25 ms after completing the algorithm. The level measurement will start 15.6 ms after the tuning algorithm, so bit LEVFLAG and the RSSI information will be updated 15.6 ms after the algorithm. The state of the TEA5766UK can be checked by reading registers: INTFLAG, FRQCHK, IFCHK and LEVCHK. Table 6 shows the possible states after an RDS update and Figure 5 shows the flowchart.

7.21.1 Muting during RDS update

An RDS update (AF jump) is always muted. There are two states after the algorithm has stopped:

1. The tuner jumps to an alternative frequency which is not valid (according to the specified SSL limit and fixed IF counter limits) and jumps back, then it will get not muted automatically.
2. The tuner jumps to a valid alternative frequency and stays there. Now it remains in mute. The host processor can switch to not muted or it keeps the tuner muted and can check for the presence of RDS data. The recommended method to get not muted is to do a preset to the current frequency (at a preset an IF count time of 15.6 ms is used, which gives a more accurate IF count result than the result obtained by the AF jump, where 2 ms is used).

Table 6. RDS update truth table[1]

Bit			Comment
IFFLAG	BLFLAG	FRRFLAG	
0	0	0	this cannot occur if INTX has gone LOW and only IFMSK, FRRMSK and BLMSK were set
0	0	1	alternative frequency jump successful; radio is tuned to the alternative frequency and keeps muted
0	1	0	not a valid state
0	1	1	not a valid state
1	0	0	not a valid state
1	0	1	AF jump has been done, but the wanted channel fails the IF count, the PLL will be set back to the old value
1	1	0	not a valid state
1	1	1	this cannot occur if INTX has gone LOW and only IFMSK, FRRMSK and BLMSK were set

[1] This table is valid until 31.25 ms after an RDS update has completed. It shows the outcome of the flag register when a read is done after INTX has gone LOW with the condition that no other mask bits are set than shown in the table.

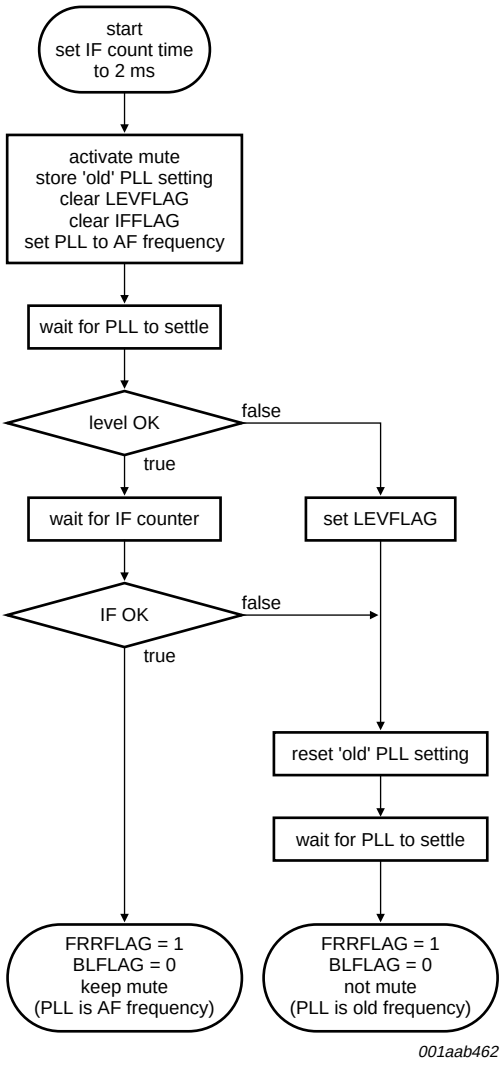


Fig 5. Flowchart RDS update

8. Interrupt handling

8.1 Interrupt register

The first two bytes of the I²C-bus register contain the interrupt masks and the interrupt flags. A flag is set when it is logic 1.

Table 7. INTFLAG (INTREQ byte 1) - I²C-bus register byte 0R bit allocation

7	6	5	4	3	2	1	0
DAVFLG	TESTBIT	LSYNCFL	IFFLAG	LEVFLAG	-	FRRFLAG	BLFLAG

Table 8. INTMSK (INTREQ byte 2) - I²C-bus register byte 1R/byte 0W bit allocation

7	6	5	4	3	2	1	0
DAVMSK	-	LSYNCMSK	IFMSK	LEVMSK	-	FRRMSK	BLMSK

The interrupt flag register contains the flags set according to the behavior outlined in Section 8.2. When these flags are set they can also cause the INTX to go active (hardware interrupt line) depending on the status of the corresponding mask bit in Table 8. A logic 1 in the mask register enables the hardware interrupt for that flag.

Hence it is conceivable that, with all the mask bits cleared, the software could operate in a polling mode by a continuous read operation of the interrupt flag register to look for bits being set.

Interrupt mask bits are always cleared after reading the first two bytes of the interrupt register. This is to control multiple hardware interrupts (see Figure 6). Bit LSYNCMSK has a different function and is not cleared after reading the interrupt register bytes (see Section 8.2.3).

8.1.1 Interrupt clearing

The interrupt flag and mask bits are always cleared after:

- They have been read via the control interface
- A power-on reset

8.1.2 Timing

The timing sequence for the general operation interrupts is shown in Figure 6 and shows a read access of the interrupt bytes INTFLAG and INTMSK and a subsequent (though not necessarily immediate) write to the mask register. It also indicates two key timing points A and B.

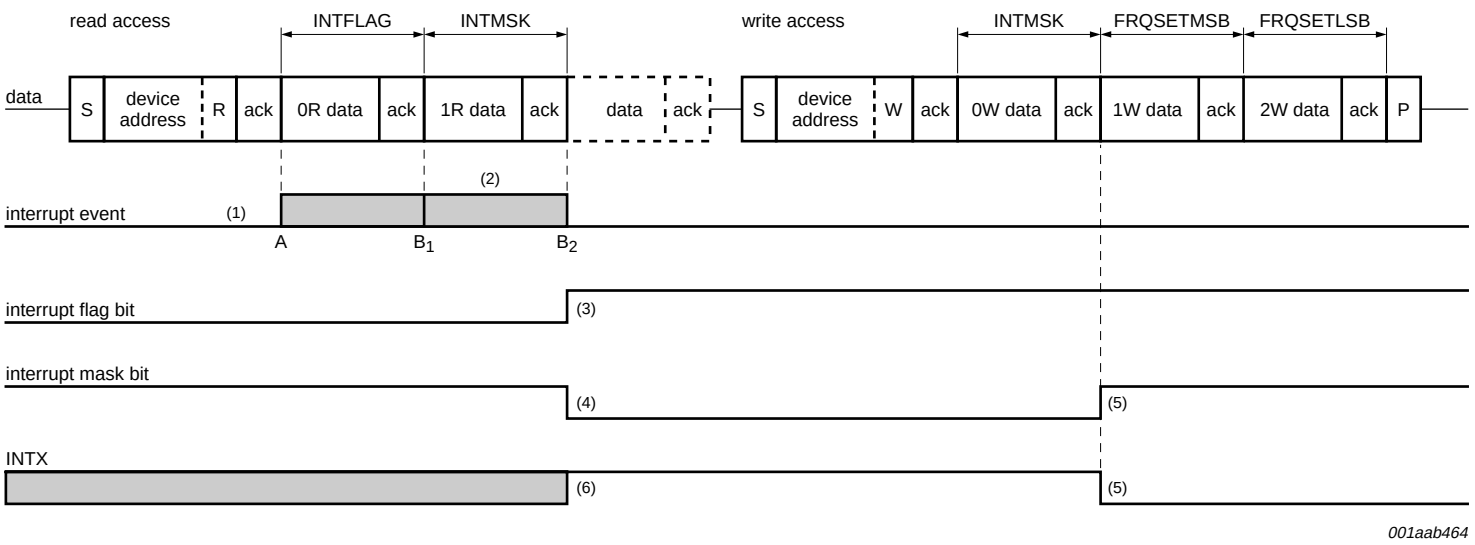
If an interrupt event occurs while the register is being accessed (after point A) it must be held until after the mask register is cleared at the end of the read operation (point B).

Point A is situated after the R/W bit has been decoded and point B is where the acknowledge has been received from the master (host processor, etc.) after the first two bytes have been sent.

The LOW time for the INTX line (t_p) has a maximum value specified in Section 13.4. However it can be shorter if the read of the INTREG registers occurs within the t_p.

8.1.3 Reset

A reset can be performed (at any time) by a simple read of the interrupt bytes (byte 0R and byte 1R), which automatically clears the interrupt flags and masks.



(1) Interrupt events that occur outside of the region A-B set their respective flag bits in the normal way immediately and can thus trigger a hardware interrupt if the mask bits are set.

(2) The blocking of interrupts is marked by the region A-B_1 / B_2 depending on the actual read cycle.

B_1 is when only the INTFLAG is read and a stop condition is received (only INTFLAG is read so only this will be cleared).

B_2 is when both registers are read and hence cleared and this is terminated by either an acknowledge or stop bit.

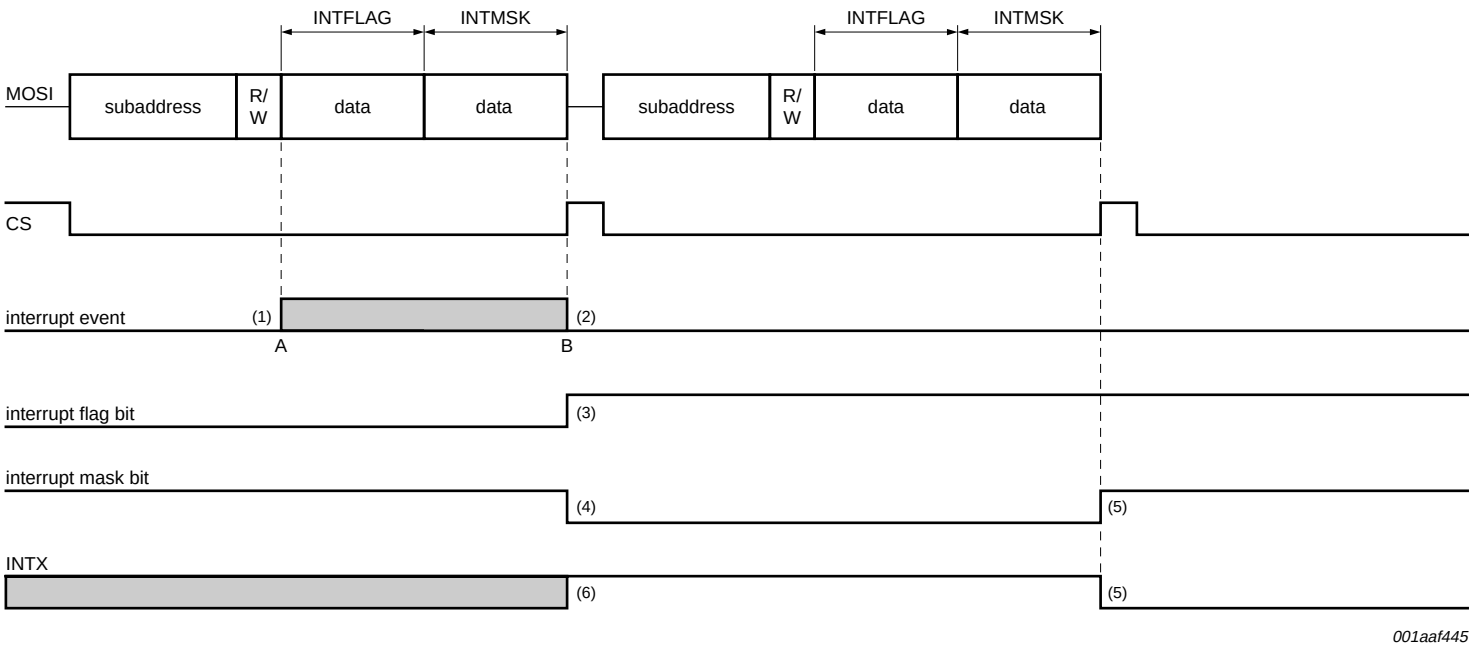
(3) Interrupt events that occur between A and B set their respective flags after the mask bits are cleared. Which means that in this diagram an interrupt event occurred in period A-B, so after A-B the flag goes to logic 1.

(4) All interrupt mask bits are cleared after the interrupt flag and mask bytes are read.

(5) Software writes to the mask byte and enables the required mask bits. Any flags currently set will then trigger a hardware interrupt.

(6) INTX is set HIGH (inactive) after the interrupt mask bytes are read.

Fig 6. I^2C-bus interrupt sequence, read and write operation



(1) Interrupt events that occur outside of the region A-B set their respective flag bits in the normal way immediately and can thus trigger a hardware interrupt if the mask bits are set.

(2) Effectively interrupts are enabled at the first falling edge of SCL after CS has gone HIGH.

(3) Interrupt events that occur between A and B set their respective flags after the mask bits are cleared, if the cause for the interrupt is still present at point B.

(4) All interrupt mask bits are cleared after the interrupt flag and mask bytes are read.

(5) Software writes to the mask register and enables the required mask bits. Any flags currently set will then trigger a hardware interrupt.

(6) INTX is set HIGH (inactive) after the interrupt flag and mask register are read.

Fig 7. SPI-bus interrupt sequence, read and write operation

8.2 Interrupt flags and behavior

8.2.1 Multiple interrupt events

If the interrupt mask register bit is set then the setting of an interrupt flag for that bit causes a hardware interrupt (INTX goes LOW). If the event occurs again before the flag is cleared, then this does not trigger any further hardware interrupts until that specific flag is cleared. However two different events can occur in sequence and generate a sequence of hardware interrupts. Only when read, followed by a write of the INTMSK byte has been done, a second interrupt can be generated, as the first interrupt blocks the input of the INTX one-shot generator.

If subsequent interrupts occur within the INTX LOW period then these interrupts do not cause the INTX period to extend beyond its specified maximum period. See also Section 8.3, Figure 8.

8.2.2 Data available: DAVFLG

When a new block of data is received, the DAVFLG is set according to the diagrams shown in Section 9 where the different DAV modes are described. Once synchronized, this continues for all subsequent received blocks (dependent on DAV mode) and in the following situations:

- During synchronization search in any DAV mode, if two valid blocks in the correct sequence are received with BBC < BBL (synchronized)
- During synchronization search in DAV-B mode if a valid A(C')-block has been detected; this mode can be used for fast search tuning (detection and comparison of the Program Identification (PI) code contained in the A(C')-block)
- If the pre-processor is synchronized and in mode DAV-A or DAV-B a new block has been processed
- If the pre-processor is synchronized and in DAV-C mode two new blocks have been processed
- If the decoder is synchronized and for any DAV mode, with LSYNCMSK = 0, loss of synchronization is detected (flywheel loss of synchronization, resulting in a restart of synchronization search)

The DAVFLG is reset by a read of BL[7:0] of RDSR2 (byte 15R) or BP[7:0] of RDSR3 (byte 17R). An interrupt is given each time when a new block of data is decoded and when the DAVMSK is set; for details see Section 9.

8.2.3 RDS synchronization: LSYNCFL

The SYNC bit, (see Table 22) shows the status of the RDS decoder. If it is set the decoder is synchronized.

The action of the TEA5766UK depends on the status of the LSYNCMSK bit in Table 8. If this is set then the loss of synchronization causes the LSYNCFL to go logic 1 and a hardware interrupt is generated. The RDS part of the TEA5766UK is set to idle and waits for the host processor to initiate a new synchronization search by setting the NWSY bit as described in Table 26.

If the LSYNCMSK bit is logic 0 and synchronization is lost the TEA5766UK automatically starts a new synchronization search. It will not generate a hardware interrupt. The host processor can wait until the RDS decoder is synchronized again; this will be indicated by the DAVFLG and the SYNC status bit (this requires the DAVMSK being set).

The LSYNCFL is reset by a read of the INTMSK byte 1R.

The LSYNCMSK is not reset by a read of the INTMSK byte; it must be set or reset by the host processor. Resetting it automatically would change the status of the TEA5766UK and cause an automatic synchronization search as described above.

How the synchronization is defined is explained in *EN 62106 Specification of the radio data system (RDS) for VHF/FM sound broadcasting range from 87.5 to 108 MHz, 1998* and in brief in Section 9.

8.2.4 IF frequency: IFFLAG

During automatic frequency search, preset or AF update, the FM part of the TEA5766UK performs a check on the received IF frequency as a measure of the level of interference in the channel received. If an incorrect IF frequency is received then this indicates the presence of strong interferers or tuning to an image and the IFFLAG bit in the INTFLAG register is set. Also a preset to a channel with no signal will result in a wrong IF count value and hence setting of the IFFLAG.

When a search, preset or AF update is finished the FRRFLAG will be set to indicate this and generates an interrupt. The host processor can now read the outcome of the registers which will contain the IF count value and the IFFLAG status of the channel it is tuned to. In case of an AF update the IF count value of the alternative frequency will be in the registers, also when it jumps back because it will then not start a new IF count. Note: 15.6 ms after the tuning algorithm has been completed the IF counter will start a new count. So 31.25 ms after a failed AF update the IF count result will be equal again to that of the channel from where the jump was initiated.

15.6 ms after the FRRFLAG has been set the IF counter will start to run continuously on the tuned frequency and if the conditions for correct frequency are not met then this sets the IFFLAG bit in the interrupt register. When the IFMSK is set this will also cause an interrupt.

The IFFLAG bit is cleared by a read of byte 1R, or by starting the tuning algorithm.

8.2.5 RSSI threshold: LEVFLAG

The level voltage reflects the field strength received by the antenna. The level voltage is analog to digital converted with 4 bits and output via the bus. This 4-bit level value can be compared to a threshold level set by the SSL bits in Table 16 or the LHSW bit in Table 19. The level ADC (which converts the analog value to digital) can be triggered to convert in two ways.

During a tuning step, a search, a preset or an AF update the LEVFLAG is triggered by these algorithms and compares the level with the threshold set by the SSL bits. The LEVFLAG bit is set if the RSSI level drops below the threshold level set by the SSL bits in Table 16 The hardware interrupt is only generated if the corresponding mask bit is set.

After a search, a preset or an AF update the threshold for comparison is switched to the hysteresis level. The hysteresis level is set by the combination of SSL bits and the LHSW bit, which results in a hysteresis as shown in Table 20. Then the level ADC starts to run automatically and compares the level each 500 μs with the hysteresis level. The LEVFLAG bit is set if the RSSI level drops below the threshold level set by the SSL bits in combination with the LHSW bit. The hardware interrupt is only generated if the corresponding mask bit is set. With the LHSW bit a small or a large hysteresis can be selected, which results in the levels of the left RSSI hysteresis threshold column for LHSW = 0 and in the right RSSI hysteresis threshold column (see Table 19).

Remark: when a search or preset is done with the ADC level set to 3 then when the algorithm has finished, the threshold level is set to 0. Hence the LEVFLAG will never be set.

The LEVFLAG bit is cleared by a read of the INTMSK byte 1R, or by starting the tuning algorithm.

8.2.6 Frequency ready: FRRFLAG

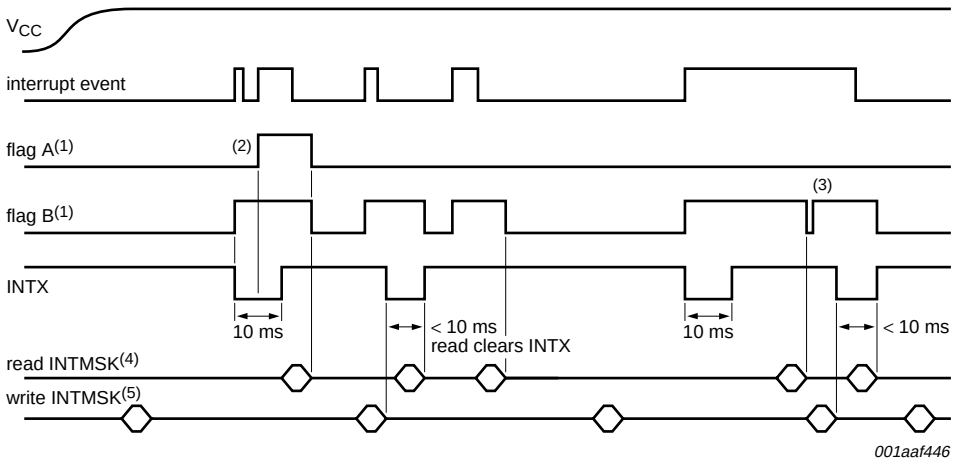
The frequency ready flag bit is set when the automatic tuning has finished a search, a preset or an RDS AF update. The function of this bit is described in Table 5 and Table 6. The FRRFLAG is cleared by a read of byte 1R.

8.2.7 Band limit: BLFLAG

The band limit bit BLFLAG is set when the automatic tuning has detected the end of the tuning band or when the PLL cannot lock on a certain frequency. The description of this bit is in Table 5 and Table 6. This bit is cleared by a read of byte 1R.

8.3 Interrupt line: pin INTX

The interrupt line driver is a MOS transistor with a nominal sink current of 900 μA, it is pulled HIGH by an 18 kΩ resistor connected to pin VREFDIG. The interrupt line can be connected to another similar device with an interrupt output and an 18 kΩ pull-up resistor, providing a wired-OR function. This allows any of the drivers to pull the line LOW by sinking the current as specified in Section 13.4. So when a flag is set and not masked it generates an interrupt.



(1) Flag is set immediately after the reset, because event is still present.

(2) When flag is set next interrupts are blocked until read or write INTMSK.

(3) When flag A is set, the interrupt is not extended beyond 10 ms.

(4) Read INTMSK clears flag, INTMSK and INTX.

(5) Write INTMSK enables INTX.

Fig 8. Interrupt line behavior

9. RDS data processing

The RDS demodulator and decoder perform the following operations:

- Demodulation of the RDS/RBDS data stream from the MPX signal
- Symbol decoding
- Obtain block and group synchronization
- Error detection and correction
- Store last and previous data block received with associated ID and error status
- Set the DAVFLG when new data is received
- Set the SYNC status bit according to the current synchronization state
- Set the LSYNCFL flag when synchronization is lost

The RDS decoder can be set in different modes, each meant to look for specific information. The modes DAV-A, DAV-B and DAV-C are described in the next paragraphs.

9.1 DAV-A processing mode

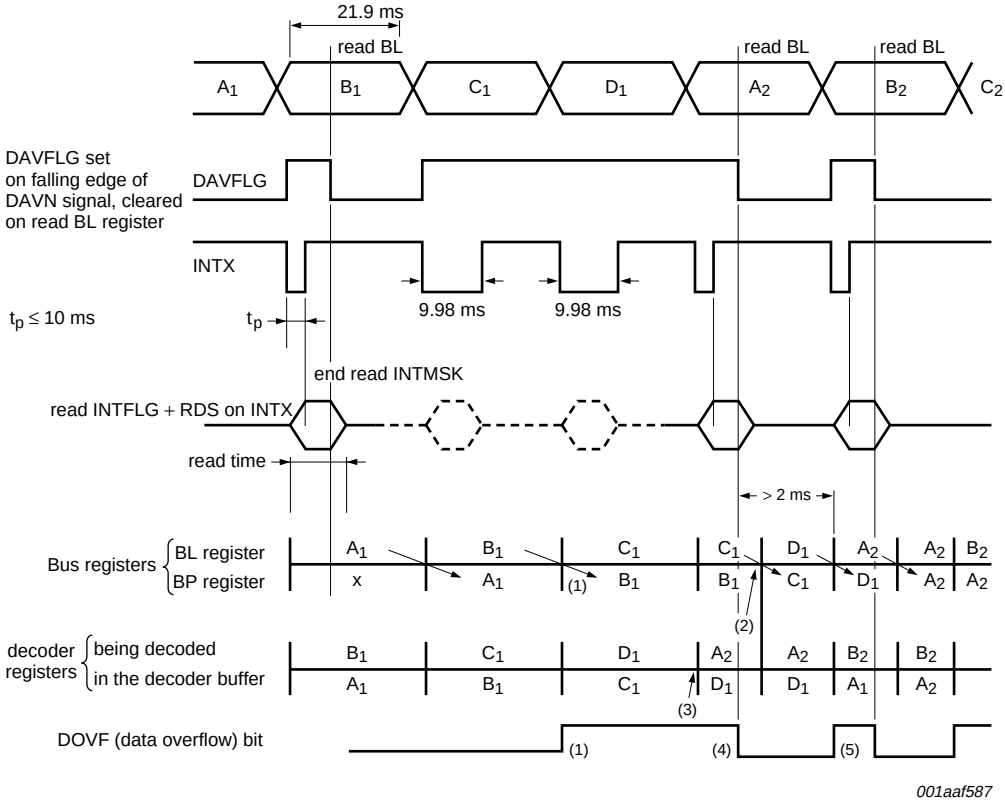
The DAV-A processing mode is the standard processing mode. In this mode each time when a data block has been decoded it is transferred to the bus registers. It generates interrupts on the INTX line after every new block of RDS data that has been processed and also the DAVFLG is set. This is shown in Figure 9. The DAVFLG is reset by a read of the bus registers.

If a data block is decoded and a new data block arrives, INTX will go LOW again, the DAVFLG will be set, the last block will be shifted to the previous block and the last decoded block will be put in the last block. This means that all RDS data is still available in the BL and BP registers.

When the bus registers are not read the DAVFLG will not be reset. If a data block is decoded and a new data block arrives, INTX will go LOW and the last block will be shifted to the previous block and the last decoded block will be put in the last block. This means that all RDS data is still available in the BL and BP registers, but must be read. This is indicated by the DOVF bit which is set.

If again the bus registers are not read, data will be lost except when this read is done within 20 ms after the INTX line has gone LOW, so 2 ms before the arrival of a new block. If this read is done at least 2 ms before the arrival of a new block, then BL and BP are read and the data in the decoder buffer is then instantaneously shifted to the BL register. All data is now read and the DOVF bit will be reset.

The diagram assumes that block synchronization has been achieved and that no other interrupt flags are being set.



(1) Bit DOVF set when 2 new blocks received in BL and BP registers.

(2) Instant copy of decoder buffer to BL register and BL to BP register after reading register RDSR4. The block in BL is considered as a new block.

(3) In order not to lose D_1 a read must be performed before D_1 enters decoder buffer, thus read finishes within 21 ms after DOVF set to logic 1.

(4) DOVF is cleared when the BL register is read. To be of use, DOVF has to be read before BL and BP registers.

(5) To prevent DOVF being set again, an extra read of BL must be performed before A2 has been decoded.

Fig 9. DAV-A timing diagram

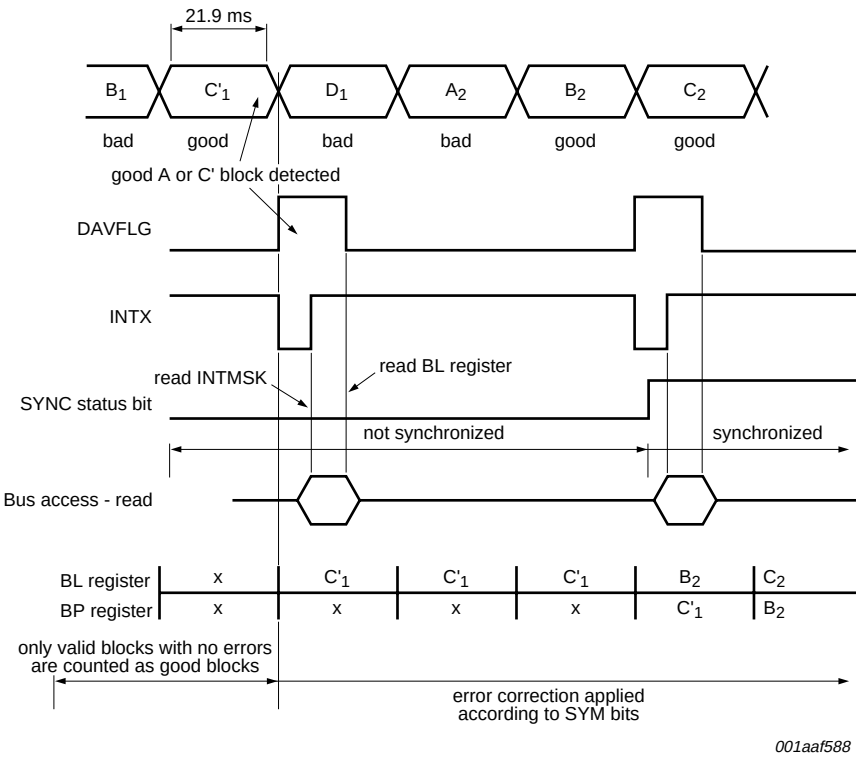
9.2 DAV-B processing mode and fast PI search mode

This mode is used when, for example, the receiver has been re-tuned to a new station and a fast search of the PI code (always contained in the A/C'-block) is required. The diagram shown in Figure 10, assumes that the RDS decoder is unsynchronized initially and is performing a synchronization search.

During synchronization search the decoder does not set the DAVFLG until a valid A/C'-block is detected. If a valid B-block is immediately detected, the decoder is synchronized and the SYNC bit is set to logic 1. In fact, if any 2 good blocks in a valid order are found the RDS decoder will synchronize and give an interrupt.

If for some reason a valid B block was not received the next valid A/C'-block is decoded and the DAVFLG set. The BP and BL registers would record the A-block history.

After synchronization each decoded block will set the DAVFLG (assuming it was reset by a read action) and generate an interrupt.

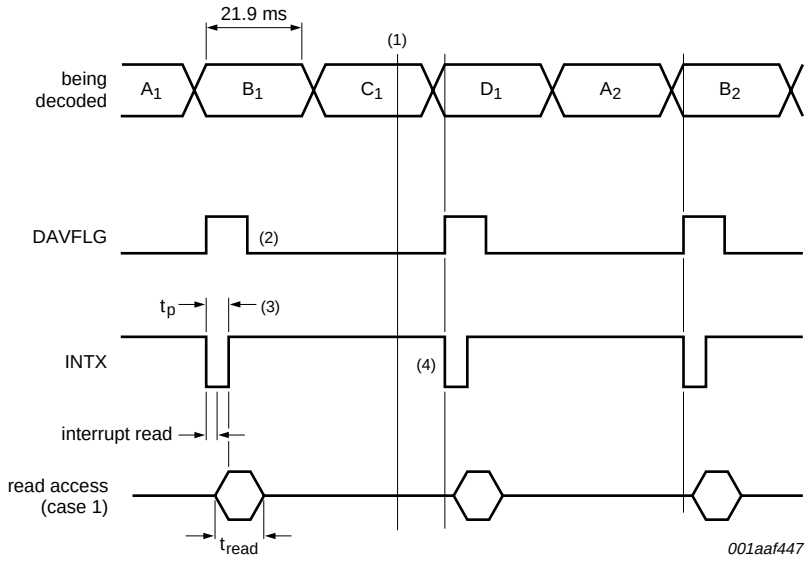


BBG = 3: synchronization is reached after receiving 1 good block and after 0, 1 or 2 bad blocks and again a good block. After three bad blocks there will be no synchronization and the counters will be reset waiting for a new good block.

Fig 10. DAV-B timing diagram

9.3 DAV-C reduced processing mode

The DAV-C processing mode is very similar to DAV-A mode with the main exception that a data flag is only set after two new blocks are received. Hence the update rate is reduced by half.



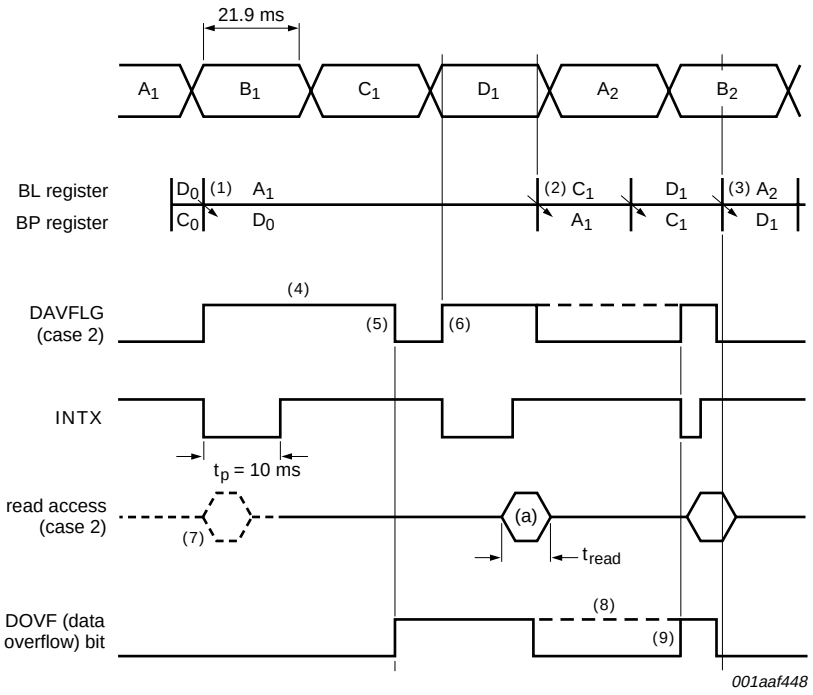
(1) B_1 is copied to the BL register shortly before C_1 is decoded.

(2) DAVFLG cleared at end read BP register and forced to zero till end read of RDSR4.

(3) INTX cleared at end read INTMSK.

(4) BL register copied to BP register and C_1 to BL register.

Fig 11. DAV-C timing diagram case 1, normal



(1) Two new blocks have arrived in the BL and BP register.

(2) Instant copy C_1 from decoder buffer to BL and BL to BP just before D_1 decoded due to read action.

(3) Instant copy of A_2 from decoder buffer to BL and BL to BP.

(4) DAVFLG not cleared as no read is performed.

(5) DAVFLG is reset when first new block would have been copied to BL register.

(6) DAVFLG is set when second new block is in decoder buffer.

(7) No read on INTX, B_1 will be lost.

(8) Dashed line shows what would happen if no read occurred at (a). DOVF bit set until the next read of BP register, however D_1 and A_2 would be lost.

(9) Two new blocks have arrived in BL/BP (C_1, D_1) and a new block (A_2) has entered the decoder buffer. Hence DOVF is set again. To prevent this, an extra read must be performed after reading (a).

Fig 12. DAV-C timing diagram case 2, late read of BL and BP register

9.4 Synchronization

9.4.1 Conditions for synchronization

When the RDS decoder is turned on it must be synchronized to extract valid data from the MPX signal. To do so the decoder automatically initiates a search for synchronization. The conditions to meet synchronization and the status of this synchronization can be set and checked with the following bits:

- BBL[5:0] - Bad Blocks Lose - these bits can be set via the bus and have a value between 0 and 63.
- GBL[5:0] - Good Blocks Lose - these bits can be set via the bus and have a value between 0 and 63.
- BBG[4:0] - Bad Blocks Gain - these bits can be set via the bus and have a value between 0 and 32.
- GBC[5:0] - Good Block Count - these bits can be read via the bus and have a value between 0 and 63.
- BBC[5:0] - Bad Block Count - bits can be read via the bus and have a value between 0 and 63.

When the decoder is not synchronized it will initiate a synchronization search. This involves calculation of the syndrome (see *EN 62106 Specification of the radio data system (RDS) for VHF/FM sound broadcasting range from 87.5 to 108 MHz, 1998* for details) for each block of 26 received bits on a bit-by-bit basis. When a correct syndrome (and hence block ID) is received the decoder clocks the next 26 bits into the internal registers and performs a second syndrome check. Synchronization is found when a certain number of blocks have been decoded and two goods blocks have been found; this number of blocks is defined by the BBG bits. If the first block needed for synchronization has been found and the expected second block (after 26 bits) is an invalid block, then the decoder module internal bad_blocks_counter is incremented and the next expected block is calculated. Exception: if RBDS mode is selected and the first block is E, then the next expected block is always block A, until synchronization is found or the maximum bad_blocks_counter value is reached. If the decoder module internal bad_blocks_counter reaches the value of the BBG[4:0], then immediately a new synchronization search (bit-by-bit) is started to find a new first block.

The synchronization is monitored by use of two flywheel counters; GBC and BBC. These are 6-bit counters that can be preset by the GBL and BBL bits to values between 0 and 63. Each time a block is decoded and recognized as a bad block the BBC value is incremented by 1. When the BBC value is equal to the BBL value, synchronization is lost. The SYNC bit will become logic 0 and the LSYNCFL is set to signal the loss of synchronization. The TEA5766UK will now automatically initiate a new synchronization search.

Each time when a good block is decoded the GBC value is incremented. When the GBC value is equal to the GBL value both counters (BBC and GBC), are set to 0 and a new count starts. The GBC counter is only incremented when the decoder is synchronized.

9.4.2 Modified Mobile Broadcast Service (MMBS) mode

There are three synchronization modes, RDS, RBDS and MMBS.

- RDS mode: the decoder can read A, B, C and D blocks and synchronize on A, B, C and D blocks.
- RBDS mode: the decoder can read A, B, C, D and E blocks and synchronize on A, B, C and D blocks.
- MMBS mode: the decoder can read A, B, C, D and E blocks and synchronize on A, B, C, D and E blocks.

MMBS mode can be selected using bit MMBS in register TESTREG (see Table 19).

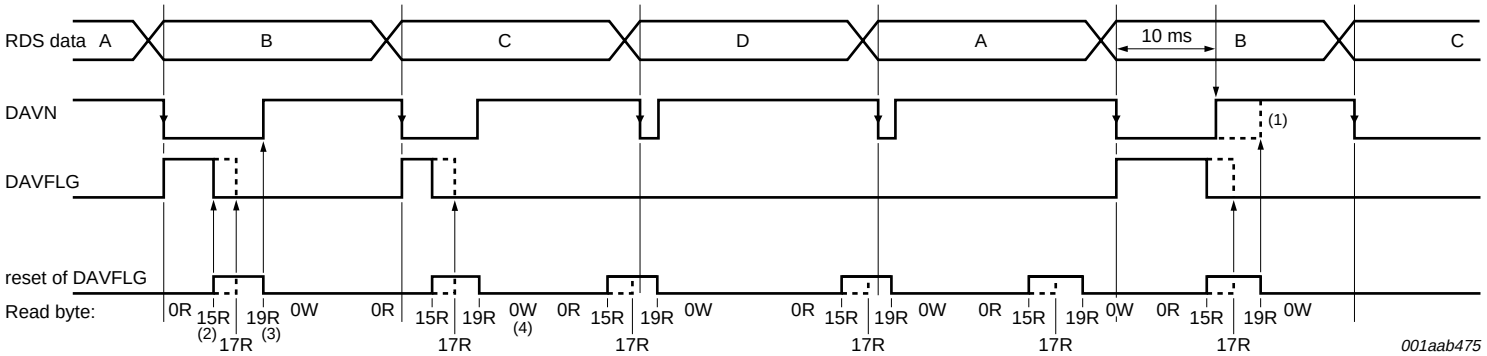
9.4.3 Data overflow

During synchronization after RDS data is read from the registers, new available blocks are shifted to the registers as described in Section 9.1 to Section 9.3. When the registers are not read in time, the decoder cannot shift any new available block to the registers and hence a data overflow will occur; this is indicated by the DOVF bit which is set to logic 1. The DOVF bit is reset by a read of the registers or if NWSY = 1 which results in the start of a new synchronization search.

9.5 RDS flag behavior during read action

Each time when an RDS data block is decoded the DAVN signal will go LOW to signal the presence of a new data block. Also the DAVN signal triggers the interrupt output INTX. In principle the microprocessor must now start reading and must have read all RDS data, so byte 12R to byte 19R before the arrival of a new RDS data block. In the application there can be a too large delay between the arrival of a new block and reading this block. This can have various causes such as a microprocessor which has to start up from Sleep mode or when polling is used instead of interrupt based read actions. Figure 13 describes the behavior of the DAVFLG and the DAVN signal when polling, which effectively means that reading can occur at any moment.

Remark: DAVN sets the INTX one-shot generator when DAVMSK = 1. Unlike INTX, DAVN is not cleared by a read of the mask register.



Blocking DAVFLG: at end of reading byte 15R or byte 17R (DAV-A, B/C) DAVFLG is forced to zero. Only after reading byte 19R DAVFLG is released again.

If synchronous reading is performed using TEA5766UK generated interrupts, this problem does not occur.

To prevent undefined situations, byte 12R to byte 19R should always be read in one action immediately after each other.

Signal DAVN ≠ INTX.

(1) Normally reading byte 19R would reset signal DAVN, but now it is reset after 10 ms, the maximal LOW time of signal DAVN.

(2) Read of byte 15R in DAV-A and DAV-B mode clears DAVFLG. In DAV-C mode two consecutive RDS data blocks are read and hence DAVFLG is reset after reading byte 17R instead of byte 15R (dotted line).

(3) Read of byte 19R clears signal DAVN.

(4) Write byte 0W (interrupt register).

Fig 13. RDS flag behavior

9.6 Error detection and reporting

The TEA5766UK must report information on the number of errors corrected in the last and previously decoded blocks. This is reported in the ELB[1:0] and EPB[1:0] fields as shown in Table 22.

During synchronization search the error correction is disabled for detection of the first block and is enabled for processing of the second block according to the mode set by the SYM[1:0] bits as described in Table 26.

9.7 RDS data - reading from registers

To read RDS data the microprocessor must read byte 12R to byte 19R. All 8 bytes must be read to reset the status bytes byte 12R and byte 13R, i.e. effectively the status bits can be updated by the decoder after reading the last bit of byte 19R. The DOVL bit is cleared after reading the last bit of byte 19R and the status of the SYNC bit does not depend on reading the register; the SYNC bit tells if the decoder is synchronized or not. When starting a read action from byte 12R, the decoder blocks update from the RDS bytes until byte 19R has been read. RDS byte 12R to byte 19R must be read in one read action.

10. Control interface

10.1 Selection between I²C-bus and SPI-bus

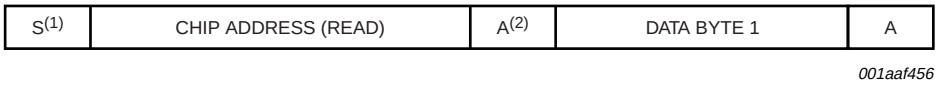
The TEA5766UK supports the I²C-bus and the 3-wire SPI-bus. With pin ISS the bus types can be selected according to Table 9.

Table 9. Bus type selection

Pin ISS	Bus
LOW	I²C-bus
HIGH	SPI 3-wire

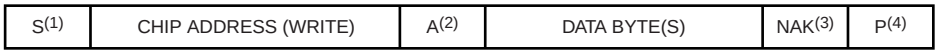
10.2 I²C-bus

The full I²C-bus specification can be found in *The I²C-bus specification, version 2.1, January 2000.*



001aaf456

a. Write mode



001aaf457

b. Read mode

(1) S = START condition.
(2) A = acknowledge (SDA LOW).
(3) NAK = non acknowledge (SDA HIGH).
(4) P = STOP condition.

Fig 14. I²C-bus data transfer

The I²C-bus specification is based on version 2.1, January 2000, expanded by the following definitions:

- The chip has two I²C-bus addresses:
  - FM radio: 001 0000[R/$\overline{W}$] starts at byte 0R or byte 0W
  - RDS part: 001 0001[R/$\overline{W}$] starts at byte 12R or byte 7W
- Structure of the I²C-bus:
  - Slave transceiver, subaddresses not used.
  - Maximum LOW-level input: $V_{IL} = 0.3 \times V_{VREFDIG}$
  - Minimum HIGH-level input: $V_{IH} = 0.7 \times V_{VREFDIG}$

10.2.1 Data transfer to the TEA5766UK

- The data transfer has to be in the order shown in Figure 14. The bit 0 (LSB) = 0 of the address indicates a WRITE operation to the TEA5766UK, indicated by the R/$\overline{W}$ bit of the I²C-bus address.
- Bit 7 of each byte is considered the MSB and has to be transferred as the first bit of the byte.
- The data becomes valid bitwise at the appropriate falling edge of the clock. A stop condition after any byte can shorten transmission times. When writing to the transceiver by using the stop condition before completion of the whole transfer:
  - The remaining bytes will contain the old information.
  - If the transfer of a byte is not completed, the new bits will be used, but a new tuning cycle will not be started.

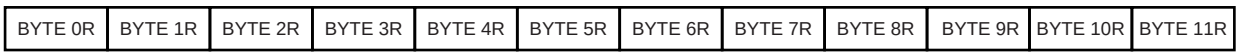
To speed up RDS traffic it is possible to read all the RDS data and then only write back byte INTMSK to set the appropriate mask(s) again.

Figure 15 shows the sequence of I²C-bus data bytes for read and write operations for both FM and FM + RDS access. For simplicity the address, start, stop and acknowledge bits are not shown. The FM and RDS part have different I²C-bus addresses as stated.

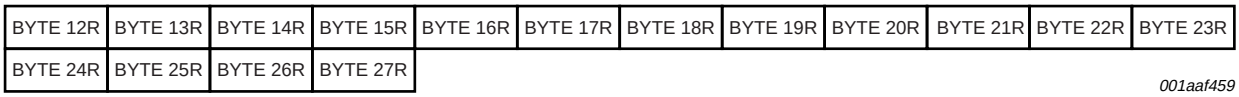
When the TEA5766UK is addressed with the FM radio address, also in one read action byte 12R to byte 27R can be read. A read does not have to stop at byte 11R.

When writing also all bytes, byte 0W to byte 10W can be written with one write action.

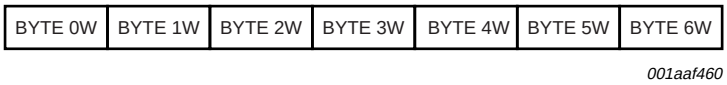
So effectively using the RDS part address only skips some bytes, which reduces bus access.



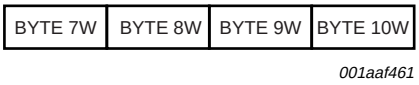
a. FM read mode data transfer



b. RDS read mode data transfer



c. FM write mode data transfer



d. RDS write mode data transfer

Fig 15. I²C-bus data transfers to the TEA5766UK

With the standby bit, the TEA5766UK can be switched in a low current Standby mode. Then the bus is still active. Is the bus interface deactivated, by making pin BUSEN LOW and without programmed Standby mode, the TEA5766UK keeps its normal operation, but is isolated from the bus lines.

It is possible to operate the TEA5766UK with pin BUSEN hard wired to pin VREFDIG and have the bus interface always active.

Power-on reset: the mute is set, all other bits are set default according to the tables in Section 11.2. To initialize the TEA5766UK all bytes have to be transferred.

10.2.2 I²C-bus output driving characteristics

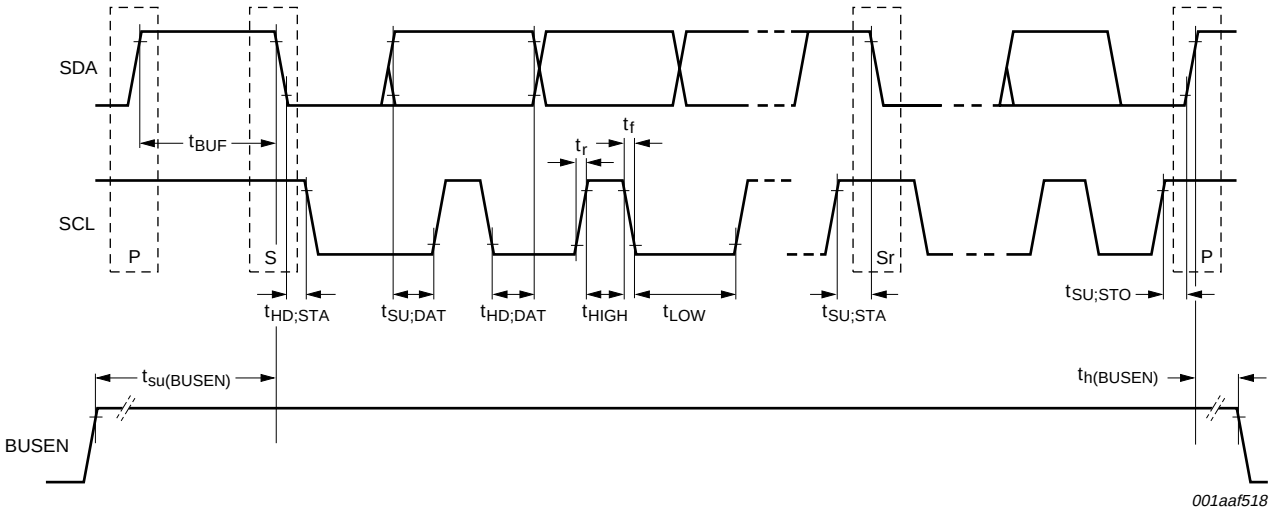
The I²C-bus output driving characteristics deviate from table 4 and table 5 in Ref. 1 as shown in Table 10.

Table 10. Characteristics of the data output stage for fast mode and standard mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL1}	LOW-level output voltage	open collector; I_{sink} = 2 mA; $V_{VREFDIG}$ > 2 V				
		standard mode	0	-	0.5	V
		fast mode	0	-	0.5	V
V_{OL3}	LOW-level output voltage	fast mode; open collector; I_{sink} = 2 mA; $V_{VREFDIG}$ < 2 V	0	-	0.5	V
t_{of}	output fall time	from $V_{IH(min)}$ to $V_{IL(max)}$; C_b = 5 pF to 100 pF [1]				
		standard mode	250	-	350	ns
		fast mode	250	-	350	ns

[1] The maximum fall time for the SDA and SCL bus lines quoted in table 5 of Ref. 1, 300 ns, is shorter than the specified maximum for the output stages, 350 ns, therefore no series protection resistors may be connected between the SDA and SCL pins and the SDA and SCL bus lines as shown in figure 36 of Ref. 1.

10.2.3 I²C-bus timing diagram



In TEA5766UK, signal SDA is present on pin DATA and signal SCL on pin CLOCK.

C_b = capacitive load for each bus line: < 100 pF.

t_f = fall time of both SDA and SCL signals: 20 + 0.1 C_b < t_f < 350 ns, where C_b = total capacitance on bus line in pF.

t_r = rise time of both SDA and SCL signals: 20 + 0.1 C_b < t_f < 350 ns, where C_b = total capacitance on bus line in pF.

$t_{HD;STA}$ = hold time (repeated) START condition. After this period, the first clock pulse is generated: > 600 ns.

t_{HIGH} = HIGH period of the SCL clock: > 600 ns.

t_{LOW} = LOW period of the SCL clock: > 1.3 µs

$t_{SU;STA}$ = set-up time for a repeated START condition: > 600 ns.

$t_{HD;DAT}$ = data hold time: 300 ns < $t_{HD;DAT}$ < 900 ns.

Remark: 300 ns lower limit is added because the TEA5766UK has no internal hold time for the SDA signal.

$t_{SU;DAT}$ = data set-up time: > 100 ns. If TEA5766UK is used in a standard mode I²C-bus system, $t_{SU;DAT}$ > 250 ns.

$t_{SU;STO}$ = set-up time for STOP condition: > 600 ns.

t_{BUF} = bus free time between a STOP and a START condition: > 600 ns.

$t_{su(BUSEN)}$ = set-up time on pin BUSEN (bus enable): > 10 µs.

$t_{h(BUSEN)}$ = hold time on pin BUSEN: > 10 µs.

Fig 16. I²C-bus timing diagram

10.3 SPI-bus

SPI stands for serial peripheral interface. TEA5766UK uses the SPI-bus in 3-wire mode, the data-in and data-out are combined to one bidirectional data line.

For this application the SPI-bus works as a slave receiver or a slave transmitter. During an SPI transfer, the input serial clock line SPICLK is driven by the master microcontroller up to a frequency of 2.5 MHz and synchronizes shifting and sampling the information on the serial data line. The slave select line CS allows individual selection of a slave SPI device. The lines of the SPI-bus interface are associated to pins as shown in Table 11.

Table 11. SPI-bus control signals and pinning

SPI signal	TEA5766UK pin	Description
CS	BUSEN	chip select (active LOW)
SPICLK	CLOCK	clock input line
MOSI/MISO	DATA	serial data input and output of slave

The TEA5766UK functions as a slave receiver and slave transmitter with a maximum clock frequency of 2.5 MHz. Data transfer is possible when signal CS (pin BUSEN) is LOW. When pin BUSEN is HIGH, the clock input line is disabled internally and the serial output of the TEA5766UK is in 3-state. The data transfer consists of packages of 8 bits data. First the address byte is shifted in, followed by 2 data bytes, which gives a total of 24 bits.

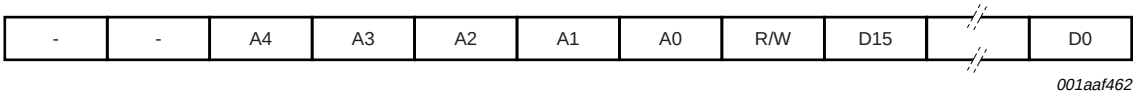


Fig 17. SPI-bus transfer

The address byte consists of 2 null bits, 5 address bits and 1 bit (R/W) for the direction of the data transfer. The 2 null bits are added to the address byte because of the SPI 8-bit data transfer protocol. Bits A[4:0] are the register address. All register addresses between 0 and 15 are allowed. Register addresses between 16 and 31 are not recognized and the SPI-bus interface leaves the data line in 3-state.

The R/W bit determines the direction of the data transfer. If R/W = 1, the slave device is set to read mode and if R/W = 0, the slave device is set to write mode.

Bits D[15:0] are the data bits. This data size corresponds to that of the register bank implemented in the TEA5766UK. The data transfer is such that the MSB is shifted first and the LSB last.

When pin BUSEN becomes LOW, an SPI start condition is detected and data is sampled in the slave device on the rising edge of the pin CLOCK signal. After the R/W bit is shifted in, the R/W selection becomes active at the next falling edge. If R/W = 1 data will be put at the data output and shifted out on the falling edge of the CLOCK.

When pin BUSEN becomes HIGH, the slave device (TEA5766UK) will be set to Idle mode, in which the data output line is set to 3-state. A negative edge on pin BUSEN restarts the data transfer. In Figure 18 and Figure 19 the SPI transfer is shown.

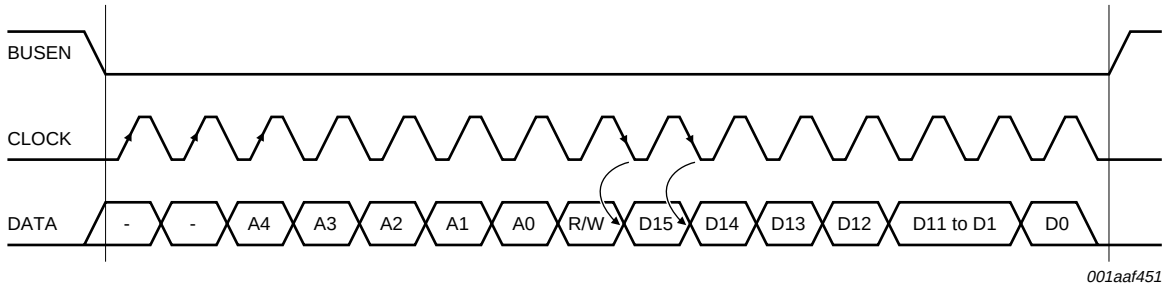
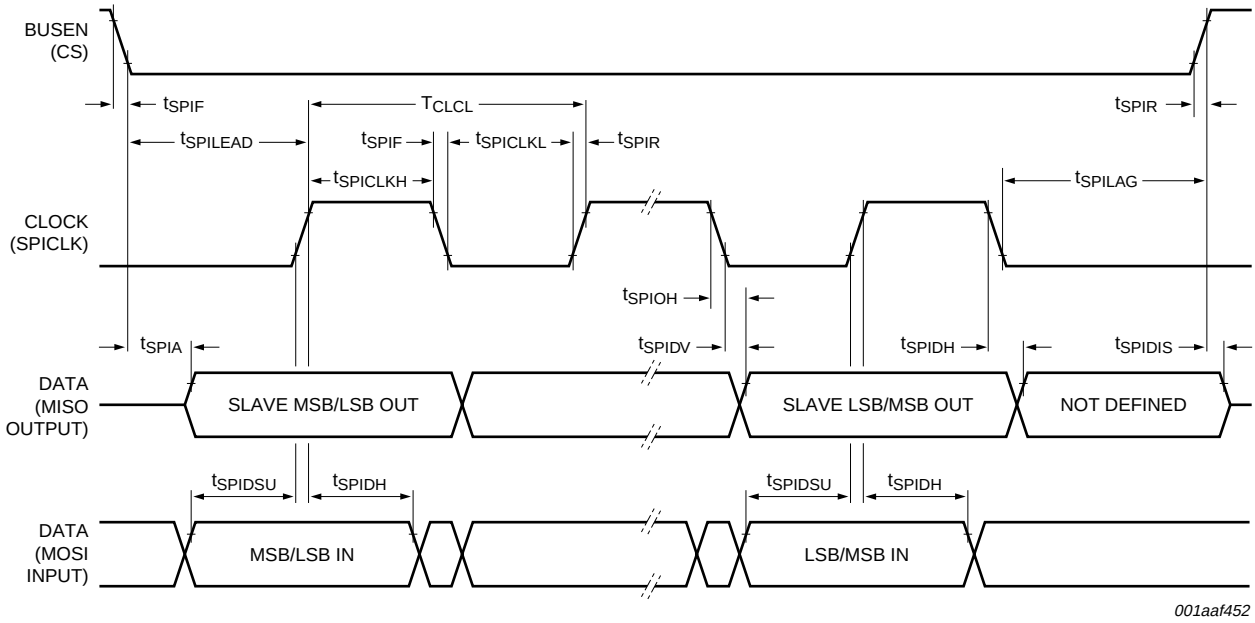


Fig 18. SPI transfer, 3 wire-mode



t_{SPIR} = SPI rise time: 5 ns < t_{SPIR} < 50 ns.

t_{SPIF} = SPI fall time: 5 ns < t_{SPIF} < 50 ns.

$t_{SPILEAD}$ = SPI enable lead time: > 250 ns.

t_{SPIA} = SPI access time (slave): > 150 ns.

T_{CLCL} = clock cycle time: > 400 ns.

$t_{SPICLKH}$ = SPICLK HIGH time: > 190 ns.

$t_{SPICLKL}$ = SPICLK LOW time: > 190 ns.

t_{SPILAG} = SPI enable lag time: > 250 ns.

t_{SPIOH} = SPI output data hold time: > 0 s.

t_{SPIDIS} = SPI disable time (slave): 0 ns < t_{SPIDIS} < 167 ns.

t_{SPIDSU} = SPI data set-up time (master or slave): > 5 ns.

t_{SPIDH} = SPI data hold time (master or slave): > 5 ns.

t_{SPIDV} = SPI enable to output data valid time: < 240 ns.

Fig 19. SPI-bus timing diagram

11. Registers

11.1 Register map

The reference for the register map is the Motorola SPI addressing. The actual register is in fact one long register, so the I²C-bus bytes are mapped onto the SPI registers.

Table 12. Register overview

Register name	SPI address	I²C-bus byte number		R/W access	Reset	Reference
		Read	Write			
INTREG	02	0R - 1R	0W[1]	R/W	0000h	Table 14
FRQSET	03	2R - 3R	1W - 2W	R/W	8000h	Table 15
TNCTRL	04	4R - 5R	3W - 4W	R/W	08D2h	Table 16
FRQCHK	05	6R - 7R		R	-	Table 17
TUNCHK	06	8R - 9R		R	-	Table 18
TESTREG	07	10R - 11R	5W - 6W	R/W	0000h	Table 19
RDSR1	08	12R - 13R		R	-	Table 22
RDSR2	09	14R - 15R		R	-	Table 23
RDSR3	10	16R - 17R		R	-	Table 24
RDSR4	11	18R - 19R		R	-	Table 25
RDSW1	12	20R - 21R	7W - 8W	R/W	0010h	Table 26
RDSW2	13	22R - 23R	9W - 10W	R/W	0000h	Table 27
MANID	00	24R - 25R		R	102Bh[2]	Table 28
CHIPID	01	26R - 27R		R	5766h	Table 29

[1] Table 13 shows how the I²C-bus bytes are mapped onto the SPI bytes.

[2] First four bits are the version bits and change with every mask set.

Table 13. SPI to I²C-bus map for SPI address 02

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI	02															
I²C	0R								1R/0W							

11.2 Register description

Table 14. INTREG - SPI address 02 or I²C byte 0R + byte 1R/byte 0W bit description

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
15	7	DAVFLG	R	0	1 = RDS data is available
14	6	TESTBIT	R	0	internal use
13	5	LSYNCFL	R	0	1 = synchronization is lost
12	4	IFFLAG	R	0	1 = IF count is not correct

Table 14. INTREG - SPI address 02 or I²C byte 0R + byte 1R/byte 0W bit description *...continued*

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
11	3	LEVFLAG	R	0	outside the tuning period the RSSI level is continuously checked: 1 = RSSI level has dropped below ADC search stop level during a tuning period (preset or search): 1 = RSSI level has dropped below ADC search stop level
10	2	-	-	0	not used
09	1	FRRFLAG	R	0	1 = the tuner state machine is ready
08	0	BLFLAG	R	0	1 = during a search the band limit has been reached or timed out
07	7	DAVMSK	R/W	0	masks bit DAVFLG
06	6	-	-	0	not used
05	5	LSYNCMSK	R/W	0	masks bit LSYNCFL
04	4	IFMSK	R/W	0	masks bit IFFLAG
03	3	LEVMSK	R/W	0	masks bit LEVFLAG
02	2	-	-	0	not used
01	1	FRRMSK	R/W	0	masks bit FRRFLAG
00	0	BLMSK	R/W	0	masks bit BLFLAG

Table 15. FRQSET - SPI address 03 or I²C byte 2R + 3R/byte 1W + byte 2W bit description

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
15	7	SUD	R/W	1	1 = search up 0 = search down
14	6	SM	R/W	0	1 = search mode 0 = preset mode
13 to 00	5 to 0 and 7 to 0	FR[13:0]	R/W	-	frequency set bits

Table 16. TNCTRL - SPI address 04 or I²C byte 4R + byte 5R/byte 3W + byte 4W bit description

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
15 and 14	7 and 6	PUPD[1:0]	R/W	0	power-up power-down 00 = FM and RDS off 01 = FM on and RDS off 10 = not used 11 = FM and RDS on
13	5	BLIM	R/W	0	1 = Japan FM band 76 MHz to 90 MHz 0 = US/Europe FM band 87.5 MHz to 108 MHz
12	4	SWPM	R/W	0	1 = software port output is bit FRRFLAG 0 = software port output is bit SWP

Table 16. TNCTRL - SPI address 04 or I²C byte 4R + byte 5R/byte 3W + byte 4W bit description *…continued*

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
11	3	IFCTC	R/W	1	1 = IF count time 15.625 ms
					0 = IF count time 2.02 ms
10	2	AFM	R/W	0	1 = L-audio and R-audio muted
					0 = audio not muted
09	1	SMUTE	R/W	0	1 = soft mute on
					0 = off
08	0	SNC	R/W	0	1 = stereo noise cancellation on
					0 = off
07	7	MU	R/W	1	1 = L-audio and R-audio muted
					0 = no hard mute
06 and 05	6 and 5	SSL[1:0]	R/W	1	search stop level
					00 = FM and RDS off
					01 = FM on and RDS off
					10 = not used
					11 = FM and RDS on
04	4	HLSI	R/W	1	1 = high-side injection
					0 = low-side injection
03	3	MST	R/W	0	1 = forced mono
					0 = stereo on
02	2	SWP	R/W	0	1 = SWPORT HIGH
					0 = SWPORT LOW
01	1	DTC	R/W	1	1 = de-emphasis time constant 50 µs
					0 = de-emphasis time constant 75 µs
00	0	AHLSI	R/W	0	1 = tuner will stop during search on failed IF count and correct level
					0 = tuner will search continuously

Table 17. FRQCHK - SPI address 05 or I²C byte 6R + byte 7R

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
15 and 14	7 and 6	-	-	-	not used
13 to 00	5 to 0 and 7 to 0	PLL[13:0]	R	-	frequency found

Table 18. TUNCHK - SPI address 06 or I²C byte 8R + byte 9R

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
15 to 09	7 to 1	IF[6:0]	R	-	IF count
08	0	TUNTO	R	-	1 = PLL tuning time-out
					0 = PLL has settled
07 to 04	7 to 4	LEV[3:0]	R	-	level count

Table 18. TUNCHK - SPI address 06 or I²C byte 8R + byte 9R *…continued*

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
03	3	LD	R	-	1 = PLL locked is detected
					0 = PLL is not locked
02	2	STEREO[1]	R	-	1 = pilot detected
					0 = no pilot
01 and 00	1 and 0	-	-	-	not used

[1] This does not switch the radio to mono or stereo. This depends on the RF input level as shown under ‘mono stereo blend’ or ‘mono stereo switched’.

Table 19. TESTREG - SPI address 07 or I²C byte 10R + byte 11R/byte 5W + byte 6W

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
15	7	LHM	R/W	0	1 = left audio output is hard muted and the radio is forced to mono
					0 = not muted
14	6	RHM	R/W	0	1 = right audio output is hard muted and the radio is forced to mono
					0 = not muted
13	5	AFMDIS	R/W	0	AFM disable bit. When AFM = 1 and TM = 1 during the tuning algorithm, AFM is disabled
12	4	LHSW	R/W	0	see Table 20
					1 = level hysteresis is large
					0 = level hysteresis is small
11	3	MMBS	R/W	0	1 = MMBS mode on
					0 = MMBS mode off
10	2	TUN	R/W	0	tuning programming error indicator when TM = 1
09	1	RFAGC	R/W	0	1 = RFAGC off
					0 = RFAGC on
08	0	INTCTRL	R/W	0	when TM = 1, INTX follows bit INTCTRL; when TM = 0, then INTCTRL = 1 generates an interrupt on INTX
07 and 06	7 and 6	-	-	-	not used
05	5	SNCLEV	R/W	0	SNCLEV switches the starting point mono/stereo blending
04	4	TM	R/W	0	1 = software Test mode and software port outputs according to Table 21
					0 = normal operation
03 to 00	3 to 0	TB[3:0]	R/W	0	test bits; Table 21 describes selection of signals available at pins SWPORT and INTX

Table 20. LH - RSSI level hysteresis

RSSI ADC search stop level	RSSI hysteresis threshold level	
	LHSW = 0	LHSW = 1
3 (SNR = 40 dBA)	0 (SNR = 0 dBA)	0 (SNR = 0 dBA)
5 (SNR = 46 dBA)	2 (SNR = 37 dBA)	1 (SNR = 34 dBA)
7 (SNR = 52 dBA)	4 (SNR = 49 dBA)	3 (SNR = 40 dBA)
10 (maximum SNR and maximum channel separation)	7 (SNR = 52 dBA)	5 (SNR = 46 dBA)

Table 21. Test bits

Test conditions: T_{amb} = 25 °C, Δf = 75 kHz including 9 % pilot, R = L, f_{mod} = 1 kHz, de-emphasis = 50 µs, MST = 0, SNC = 1, IEC filter (200 Hz to 15 kHz), A-weighting filter.

TB3	TB2	TB1	TB0	Output signal	Pin	Bit TM
0	0	0	0	bit SWP of byte 4W, depending on bits SWPM and SWP or FRRFLAG	SWPORT	0 or 1
0	0	0	1	oscillator output 32.768 kHz	SWPORT	1
0	0	1	0	lock detect bit LD	SWPORT	1
0	0	1	1	pilot detected signal	SWPORT	1
0	1	0	0	programmable divider	SWPORT	1
0	1	0	1	INTX output equal to INTCTRL; pin SWPORT = LOW	INTX	1
0	1	1	0	3.8 MHz clock	SWPORT	1

Table 22. RDSR1 - SPI address 08 or I²C byte 12R + byte 13R

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
15	7	-	-	-	not used
14 to 12	6 to 4	BLID[2:0]	R	-	block ID of last block
					000 = A
					001 = B
					010 = C
					011 = D
					100 = C'
					101 = E
					110 = invalid block E (RBDS)
					111 = invalid block
11 and 10	3 and 2	-	-	-	not used
09 and 08	1 and 0	ELB[1:0]	R	-	number of errors for last processed block
					00 = no errors
					01 = maximum 2 bits
					10 = maximum 5 bits
					11 = uncorrectable

Table 22. RDSR1 - SPI address 08 or I²C byte 12R + byte 13R *…continued*

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
07 to 05	7 to 5	BPID[2:0]	R	-	block ID of previous block
					000 = A
					001 = B
					010 = C
					011 = D
					100 = C'
					101 = E
					110 = invalid block E (RBDS)
					111 = invalid block
04 and 03	4 and 3	EPB[1:0]	R	-	number of errors for previous processed block
					00 = no errors
					01 = maximum 2 bits
					10 = maximum 5 bits
					11 = uncorrectable
02	2	SYNC	R	-	1 = RDS bitstream is synchronized
					0 = not synchronized
01	1	RSTD	R	-	1 = power-on reset detected
00	0	DOVF	R	-	1 = data overflow occurred during read operation
					0 = normal operation

Table 23. RDSR2 - SPI address 09 or I²C byte 13R + byte 15R

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
15 to 00	7 to 0 and 7 to 0	BL[15:0]	R	-	last RDS data byte

Table 24. RDSR3 - SPI address 10 or I²C byte 16R + byte 17R

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
15 to 00	7 to 0 and 7 to 0	BP[15:0]	R	-	previous RDS data byte

Table 25. RDSR4 - SPI address 11 or I²C byte 18R + byte 19R

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
15 to 10	7 to 2	BBC[5:0]	R	-	bad block count
09 to 04	1 to 0 and 7 to 4	GBC[5:0]	R	-	good block count
03 to 00	3 to 0	-	-	-	not used

Table 26. RDSW1 - SPI address 12 or I²C byte 20R + byte 21R/byte 7W + byte 8W

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
15	7	NWSY	R/W	0	1 = start new synchronization
					0 = normal processing
14 and 13	6 and 5	SYM[1:0]	R/W	0	error correction
					00 = no correction
					01 = maximum 2 bits
					10 = maximum 5 bits
					11 = no correction
12	4	RBDS	R/W	0	1 = RBDS processing mode
					0 = RDS processing mode
11 and 10	3 and 2	DAC[1:0]	R/W	0	RDS data output mode
					00 = DAV-A
					01 = DAV-B
					10 = DAV-C
					11 = not used
09 to 05	1 and 0; 7 to 5	-	-	-	not used
04 to 00	4 to 0	BBG[4:0]	R/W	1 0000	bad blocks gain

Table 27. RDSW2 - SPI address 13 or I²C byte 22R + byte 23R/byte 9W + byte 10W

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
15 to 12	7 to 4	-	-	-	not used
11 to 06	3 to 0; 7 and 6	GBL[5:0]	R/W	0	these bits set the maximum number of good blocks
05 to 00	5 to 0	BBL[5:0]	R/W	0	these bits set the maximum number of bad blocks

Table 28. MANID - SPI address 00 or I²C byte 24R + byte 25R

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
15 to 12	7 to 4	VERSION[3:0]	R	-	version code = 0001h
11 to 01	3 to 0; 7 to 2	MANID[10:0]	R	-	manufacturer ID code = 015h
00	0	IDAV	R	1	1 = manufacturer ID available in I²C-bus mode
					0 = chip has no ID

Table 29. CHIPID - SPI address 01 or I²C byte 26R + byte 27R

Bit		Symbol	Access	Reset value	Description
SPI	I²C				
15 to 00	7 to 0; 7 to 0	CHIPID[15:0]	R	-	chip identification code = 5766h

12. Limiting values

Table 30. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{LO1}	voltage on pin LO1			–0.6	+4.5	V
V_{LO2}	voltage on pin LO2			–0.6	+4.5	V
V_{CCD}	digital supply voltage			–0.6	+4.5	V
V_{CCA}	analog supply voltage			–0.6	+4.5	V
V_I	input voltage	with respect to ground		–0.6	+4.5	V
V_O	output voltage	with respect to ground		–0.6	+4.5	V
T_{stg}	storage temperature			–40	+125	°C
T_{amb}	ambient temperature	TEA5766UK functional, specification not guaranteed		–30	+85	°C
V_{esd}	electrostatic discharge voltage	machine model	[1]	–200	+200	V
		human body model	[2]			
		pin SWPORT		–2000	+500	V
		any other pin		–2000	+2000	V
		charged device model	[3]	–500	+500	V

[1] Machine model (L = 0.75 mH, R = 10 Ω, C = 200 pF).

[2] Human body model (R = 1.5 kΩ, C = 100 pF).

[3] Charged device model; see *JEDEC Standard JESD22-C101C*.

13. Characteristics

13.1 General characteristics

Table 31. General characteristics

Under all conditions a reference clock of 32.768 kHz is present.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CCA}	analog supply voltage			2.6	2.7	3.6	V
$V_{CC(VCO)}$	VCO supply voltage			2.6	2.7	3.6	V
I_{CCA}	analog supply current	operating	[1]	-	13.5	17	mA
		Standby mode	[1]	-	-	5	µA
V_{CCD}	digital supply voltage			2.6	2.7	3.6	V
I_{CCD}	digital supply current	operating; RDS off		-	350	450	µA
		operating; RDS on		-	0.75	1.5	mA
		Standby mode		-	5	10	µA
		Sleep mode; only in I^2C-bus; BUSEN = HIGH		-	16	25	µA
$V_{VREFDIG}$	voltage on pin VREFDIG	$V_{VREFDIG} \leq V_{CCD}$		1.65	1.8	V_{CCD}	V

Table 31. General characteristics *...continued*

Under all conditions a reference clock of 32.768 kHz is present.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VREFDIG}$	current on pin VREFDIG		0	0.5	1	µA
		Standby mode	0	0.5	1	µA
$f_{i(FM)}$	FM input frequency		76	-	108	MHz
T_{amb}	ambient temperature	device meets all specifications	–20	-	+85	°C

[1] Includes both analog supply current on pin V_{CCA} and VCO supply current on pin $V_{CC(VCO)}$.

13.2 Reference clock

The electrical characteristics as stated in Section 13.4 are valid under restriction of the reference clock as specified in Table 32.

Table 32. Reference clock definition, pin FREQIN

Reference clock 32.768 kHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f	frequency	T_{amb} = 25 °C	-	32.768	-	kHz
Δf/f	relative frequency difference	T_{amb} = 25 °C	-20×10^{-6}	-	$+20 \times 10^{-6}$	
		T_{amb} = –20 °C to +85 °C	-150×10^{-6}	-	$+150 \times 10^{-6}$	
δ	duty cycle	square wave	30	-	70	%
t_r	rise time		5	-	50	ns
t_f	fall time		5	-	50	ns
V_{IH}	HIGH-level input voltage	square wave	1.1	-	V_{CCD}	V
V_{IL}	LOW-level input voltage	square wave	0	-	0.7	V
f_{jit}	frequency jitter	integrated over 200 Hz to 15000 Hz	-	-	1	Hz

13.3 Audio measurement filter

The IEC filter referenced to in the electrical characteristics of Section 13.4 is defined in IEC 60315-4. The audio bandwidth of this filter lies between 200 Hz and 15 kHz.

13.4 Characteristics

Table 33. Characteristics

All AC values are given in RMS unless otherwise specified. The min and max values include spread due to:
V_{CC} = 2.6 V to 3.6 V; T_{amb} = –20 °C to +85 °C, reference frequency offset + deviation and process spread.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Antenna input including matching circuit						
Z_i	input impedance	f_{RF} = 76 MHz to 108 MHz	-	50	-	Ω
$\|s_{11}\|^2$	input return loss	f_{RF} = 76 MHz to 108 MHz	–5	-	-	dB
Voltage controlled oscillator						
f_{VCO}	VCO frequency		150	-	217	MHz
Reference frequency input, pin FREQIN						
V_{FREQIN}	voltage on pin FREQIN	switching level	0.7	0.925	1.1	V
R_i	input resistance		1	-	-	MΩ

Table 33. Characteristics *...continued*

All AC values are given in RMS unless otherwise specified. The min and max values include spread due to:
V_{CC} = 2.6 V to 3.6 V; T_{amb} = −20 °C to +85 °C, reference frequency offset + deviation and process spread.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance		-	-	7	pF
Synthesizer						
t_s	settling time	single frequency jump in any direction to a frequency within the frequency band (87.5 MHz to 108 MHz or 76 MHz to 90 MHz); settling limit is ±5 kHz of target frequency	-	-	50	ms
D_{prog}	programmable divider	FRQSET[15:8] = XX01 1111; FRQSET[7:0] = 1111 1111	-	-	8191	
		FRQSET[15:8] = XX00 1000; FRQSET[7:0] = 0000 0000	2048	-	-	
$D_{prog(step)}$	programmable divider step		-	1	-	
f_{step}	step frequency		-	100	-	kHz
IF counter						
N_{IFc}	IF counter length		-	7	-	bit
V_{sens}	sensitivity voltage		-	-	3[1]	µV
$N_{IFc(result)}$	IF counter result	for search stop; stop level voltage < V_{RF} < 2 V[1]	31h	-	3Ch	
			49	-	60	
T	period	16 ms; IFCTC = 1	-	15625	-	µs
		2 ms; IFCTC = 0	-	1953	-	µs
$N_{IFc(res)}$	IF counter resolution		-	4096	-	Hz
Logic pins: BUSEN, CLOCK, DATA and BUSMODE						
R_i	input resistance		2.5	-	-	MΩ
V_{IH}	HIGH-level input voltage		0.7 × $V_{VREFDIG}$	-	$V_{VREFDIG}$ + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	0.3 × $V_{VREFDIG}$	V
Logic pin: data output SPI mode						
V_{OL}	LOW-level output voltage	I_{load} = 2 mA	0	-	0.22 × $V_{VREFDIG}$	MΩ
V_{OH}	HIGH-level output voltage	I_{load} = 2 mA	0.8 × $V_{VREFDIG}$	-	$V_{VREFDIG}$	V
$t_{r(o)}$	output rise time	C_L < 10 pF	5	-	20	ns
$t_{f(o)}$	output fall time	C_L < 10 pF	5	-	20	ns
Software programmable port pin: SWPORT						
$V_{O(max)}$	maximum output voltage	I_{load} = 150 µA	$V_{VREFDIG}$ − 0.25	-	$V_{VREFDIG}$	V
$V_{O(min)}$	minimum output voltage	I_{load} = 150 µA	0	0.2	0.45	V
I_{sink}	sink current	V_{SWPORT} = 1.8 V	0.75	1.8	5	mA
I_{source}	source current	V_{SWPORT} = 0 V	0.75	1.8	5	mA

Table 33. Characteristics *...continued*

All AC values are given in RMS unless otherwise specified. The min and max values include spread due to: V_{CC} = 2.6 V to 3.6 V; T_{amb} = −20 °C to +85 °C, reference frequency offset + deviation and process spread.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pin INTX						
$V_{O(max)}$	maximum output voltage	$V_{VREFDIG} \geq 1.65$ V; pull-up resistor of second device connected to INTX is 18 kΩ ± 20 %	$V_{VREFDIG} - 0.2$	-	$V_{VREFDIG} + 0.2$	V
$V_{O(min)}$	minimum output voltage		0	-	$0.22 \times V_{VREFDIG}$	V
I_{source}	source current	including $R_{pu(int)}$	700	900	1100	µA
$R_{pu(int)}$	internal pull-up resistance		14.4	18	24	kΩ
t_p	pulse duration		9	-	10	ms
FM RF input						
V_{sens}	sensitivity voltage	f_{RF} = 76 MHz to 108 MHz; Δf = 22.5 kHz; f_{mod} = 1 kHz; (S+N/N) = 26 dB; de-emphasis = 50 µs; L = R; IEC filter + A-weighting filter	-	2[1]	3[1]	µV
S/N	signal-to-noise ratio	f_{RF} = 76 MHz to 108 MHz; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 50 µs; L = R; V_{RF} = 10 µV[1]; IEC filter + A-weighting filter	45	-	-	dBA
$IP3_{ib}$	in-band third-order intercept point	Δf_1 = 200 kHz; Δf_2 = 400 kHz; f_{tune} = 76 MHz to 108 MHz	82	95	-	dBµV
$IP3_{ob}$	out-band third-order intercept point	Δf_1 = 4 MHz; Δf_2 = 8 MHz; f_{tune} = 76 MHz to 108 MHz	88	100	-	dBµV
IF filter						
f_c	center frequency		217	221	233	kHz
S_{200}	200 kHz selectivity	$\Delta f = \pm 200$ kHz; f_{RF} = 76 MHz to 108 MHz; measured according to EN 55020; de-emphasis 50 µs	16	-	-	dB
S_{FM}	FM selectivity	Δf = 300 kHz minimum; f_{RF} = 76 MHz to 108 MHz; except image frequency band; measured according to EN 55020; de-emphasis 50 µs	35	-	-	dB
$\alpha_{f(image)}$	image frequency rejection	Δf = 450 kHz; measured according to EN 55020; image rejection defined as difference between image and co-channel response; de-emphasis 50 µs	25	-	-	dB
FM IF level detector and mute voltage, see Figure 20						
ΔG	gain deviation	deviation from average curve	−2	-	+2	dB
$V_{ADC(start)}$	start ADC voltage	extrapolated	0.75[1]	1.6[1]	2.5[1]	µV
$G_{ADC(step)}$	step of ADC gain	average	2.5	2.8	3	dB
Soft mute						
$V_{mute(start)}$	start mute voltage	SMUTE = 1	2	3.5	5	µV

Table 33. Characteristics *...continued*

All AC values are given in RMS unless otherwise specified. The min and max values include spread due to: V_{CC} = 2.6 V to 3.6 V; T_{amb} = −20 °C to +85 °C, reference frequency offset + deviation and process spread.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{mute}	mute attenuation	V_{RF} = 1.26 µV[1]; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs; IEC filter; SMUTE = 1	5	5.8	8	dB
Stereo decoder, pins VAFL and VAFR						
V_O	output voltage	V_{RF} = 2 mV[1]; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	60	75	90	mV
R_O	output resistance	MU = LHM = RHM = 0; AFM = 0 or AFM = 1	250	350	400	Ω
		hard mute; MU = LHM = RHM = 1; AFM = 0 or AFM = 1	500	-	-	kΩ
		Standby mode; PUPD0 = 0	1	-	-	MΩ
I_O	output current	minimum load resistance = 10 kΩ	80	100	120	µA
$\|G_v\|$	voltage gain difference	V_{RF} = 2 mV[1]; L = R; Δf = 75 kHz; f_{mod} = 1 kHz; IEC filter; de-emphasis = 75 µs	−0.5	-	+0.5	dB
$\alpha_{cs(stereo)}$	stereo channel separation	V_{RF} = 2 mV[1]; Δf = 75 kHz including 9 % pilot; R= 0 and L= 1 or R= 1 and L= 0; f_{mod} = 1 kHz; IEC filter; MST = 0; SNC = 0 or SNC = 1 + SNCLEV = 1	27	45	-	dB
$f_{-3dB(l)}$	low frequency −3 dB point	V_{RF} = 2 mV[1]; Δf = 22.5 kHz; L = R; pre-emphasis = 75 µs; de-emphasis = 75 µs	-	-	20	Hz
$f_{-3dB(h)}$	high frequency −3 dB point	V_{RF} = 2 mV[1]; Δf = 22.5 kHz; L = R; pre-emphasis = 75 µs; de-emphasis = 75 µs	15	-	-	kHz
(S+N)/N	signal plus noise-to-noise ratio	V_{RF} = 2 mV[1]; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 50 µs; IEC filter + A-weighting filter				
		mono	53	57	-	dBA
		stereo; Δf_{pilot} = 6.75 kHz	49	53	-	dBA
$\alpha_{resp(sp)}$	spurious response	relative to Δf = 22.5 kHz; f_{mod} = 1 kHz (mono); V_{RF} = 2 mV[1]; de-emphasis = 50 µs; IEC filter + A-weighting filter	-	-	−60	dB

Table 33. Characteristics *...continued*

All AC values are given in RMS unless otherwise specified. The min and max values include spread due to: V_{CC} = 2.6 V to 3.6 V; T_{amb} = −20 °C to +85 °C, reference frequency offset + deviation and process spread.

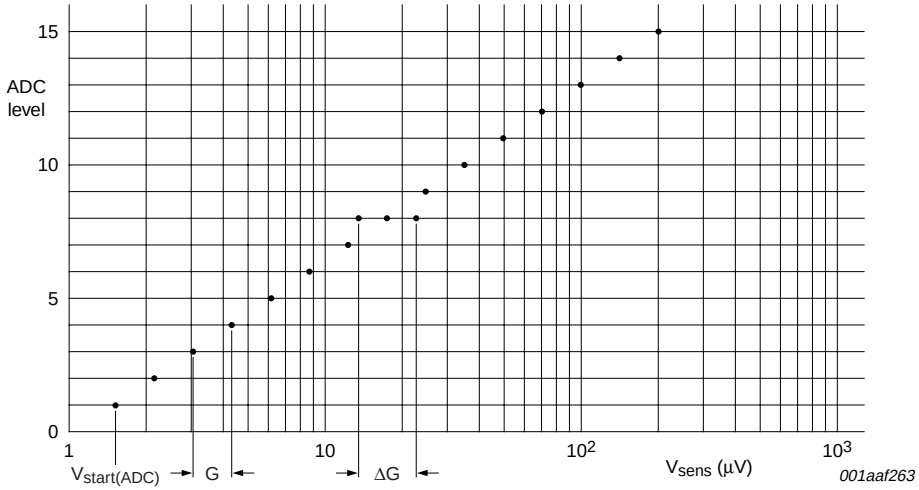
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
THD	total harmonic distortion	mono; V_{RF} = 2 mV[1]; L = R; de-emphasis = 75 µs					
		Δf = 75 kHz; f_{mod} = 400 Hz		-	0.4	0.8	%
		Δf = 75 kHz; f_{mod} = 1 kHz		-	0.4	0.8	%
		Δf = 75 kHz; f_{mod} = 3 kHz		-	0.4	0.8	%
		Δf = 100 kHz; f_{mod} = 1 kHz		-	0.5	1	%
		stereo; V_{RF} = 2 mV[1]; Δf = 75 kHz; L = R including 9 % pilot; de-emphasis = 75 µs					
		f_{mod} = 1 kHz		-	0.5	1.5	%
		f_{mod} = 3 kHz		-	0.5	1.5	%
α_{AM}	AM suppression	L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; m = 0.3; de-emphasis = 75 µs; IEC filter; A-weighting filter					
		V_{RF} = 20 µV	[1]	40	-	-	dB
		V_{RF} = 200 µV to 20 mV	[1]	45	-	-	dB
α_{pilot}	pilot suppression	related to Δf = 75 kHz; including 9 % pilot; L = 0 and R = 1 or L = 1 and R = 0; f_{mod} = 1 kHz; de-emphasis = 75 µs		40	50	-	dB
Δf_{pilot}	pilot frequency deviation	stereo; required for pilot detection; V_{RF} = 2 mV	[1]	1.8	3.6	5.8	kHz
$\alpha_{hys(pilot)}$	pilot hysteresis	V_{RF} = 2 mV	[1]	2	2.5	4	dB
τ_{deemp}	de-emphasis time constant	DTC = 1 (50 µs)		40	50	60	µs
		DTC = 0 (75 µs)		60	75	90	µs
Mono stereo blend							
$V_{start(blend)}$	blend start voltage	stereo channel separation = 1 dB; SNC = 1					
		SNCLEV = 0		8[1]	12[1]	20[1]	µV
		SNCLEV =1		4[1]	6[1]	10[1]	µV
$\alpha_{cs(stereo)}$	stereo channel separation	V_{RF} = 70 µV[1]; Δf = 75 kHz; R = 0 and L = 1 or R = 1 and L = 0; including 9 % pilot; f_{mod} = 1 kHz; MST = 0; SNC = 1; SNCLEV = 0		8	12	18	dB
Mono stereo switched							
V_{sw}	switch voltage	Δf = 75 kHz; including 9 % pilot; f_{mod} = 1 kHz; SNC = 0; spread due to RSSI variation		65[1]	90[1]	115[1]	µV
$\lvert\Delta V_{sw}/V_{sw}\rvert$	switch voltage deviation over switch voltage ratio	Δf = 75 kHz; including 9 % pilot; f_{mod} = 1 kHz; SNC = 0		2	3	4	dB

Table 33. Characteristics *...continued*

All AC values are given in RMS unless otherwise specified. The min and max values include spread due to: V_{CC} = 2.6 V to 3.6 V; T_{amb} = −20 °C to +85 °C, reference frequency offset + deviation and process spread.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Mute functions						
α_{mute}	mute attenuation	Δf = 75 kHz; mono; IEC filter				
		AFM = 1 or RHM = 1; LHM = 0	-	-	−60	dB
		AFM = 1 or LHM = 1; RHM = 0	-	-	−60	dB
		MU = 1	-	-	−80	dB
RDS filter/demodulator/decoder						
V_{sens}	sensitivity voltage	f_{RF} = 87.5 MHz to 108 MHz; Δf = 22.5 kHz; f_{AF} = 1 kHz; L = R; Δf_{RDS} = 2 kHz; block quality rate ≥ 95 %; SYM1 = 0 and SYM0 = 0; average over 2000 blocks	-	14[1]	20[1]	μV
f_c	center frequency		56	57	58	kHz
B	bandwidth		2.5	3	3.5	kHz

[1] EMF value.



$V_{ADC(start)}$ is the starting point of the curve. Taking the starting point the curve shows a monotone increase, increasing with the average step size $G_{ADC(step)}$. The maximum deviation from the average curve is ΔG.

Fig 20. FM IF level detector and mute voltage

14. Application information

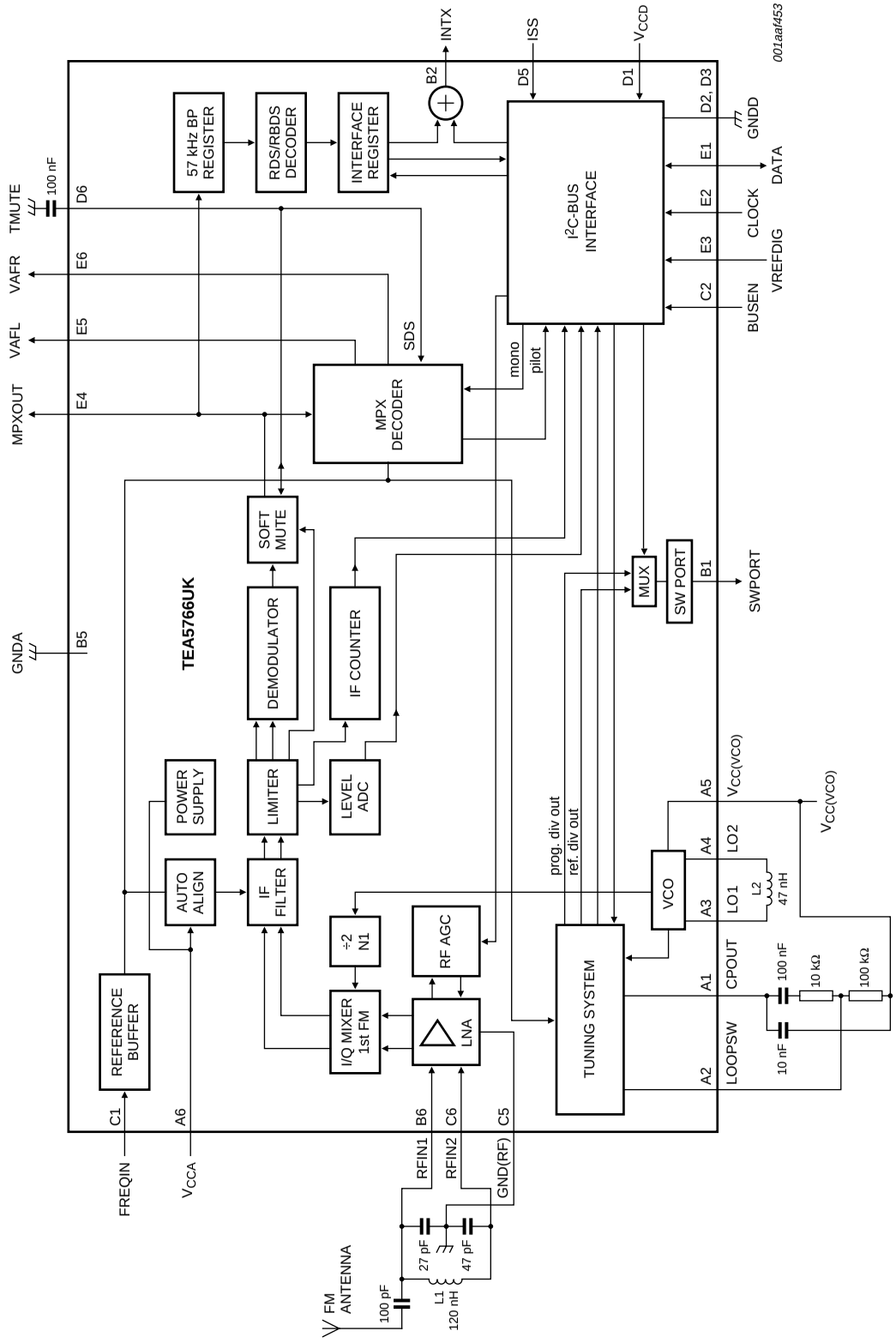


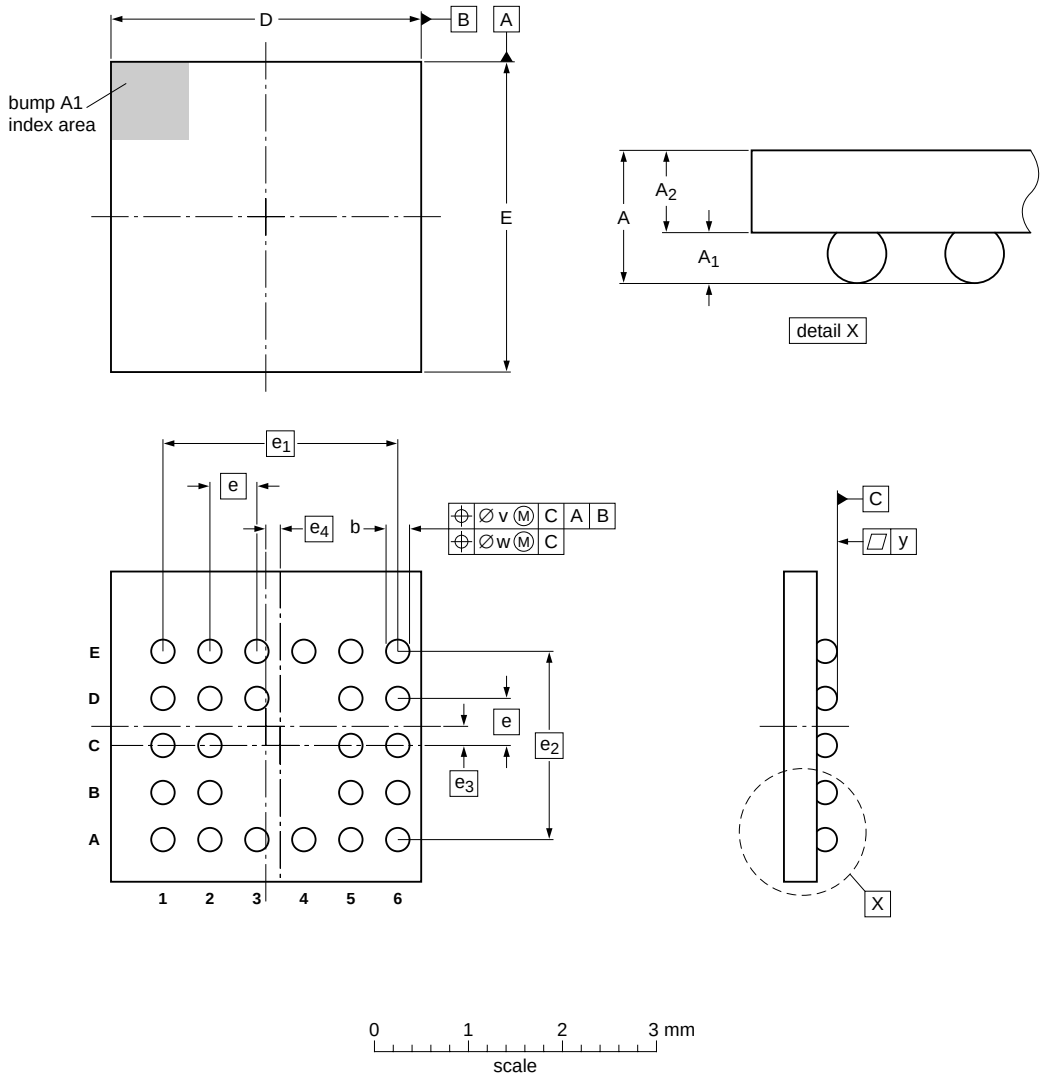
Fig 21. Application diagram

Table 34. List of components

Symbol	Parameter	Type
L1	120 nH	Murata LQW15ANR12J00 or equivalent, Qmin = 20 (f = 100 MHz), tolerance ±5 %
L2	47 nH	Murata LQW15AN47NJ00 or equivalent, Qmin = 25 (f = 250 MHz), tolerance ±5 %
R	10 kΩ and 100 kΩ	tolerance ±10 % maximum
C	27 pF, 47 pF, 100 pF, 10 nF and 100 nF	tolerance ±10 % maximum

15. Package outline

WLCSP25: wafer level chip-size package; 25 bumps; 3.3 x 3.25 x 0.6 mm **TEA5766**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	e_3	e_4	v	w	y
mm	0.64	0.26 0.22	0.38 0.34	0.34 0.30	3.35 3.30	3.30 3.25	0.5	2.5	2	0.2	0.15	0.01	0.04	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
TEA5766						~~06-02-23~~ 06-03-03

Fig 22. Package outline TEA5766 (WLCSP25)

16. Soldering

16.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in Application Note *AN10439 "Wafer Level Chip Scale Package"* and in *Application Note AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

16.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

16.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 23) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 35 and 36

Table 35. SnPb eutectic process (from J-STD-020C)

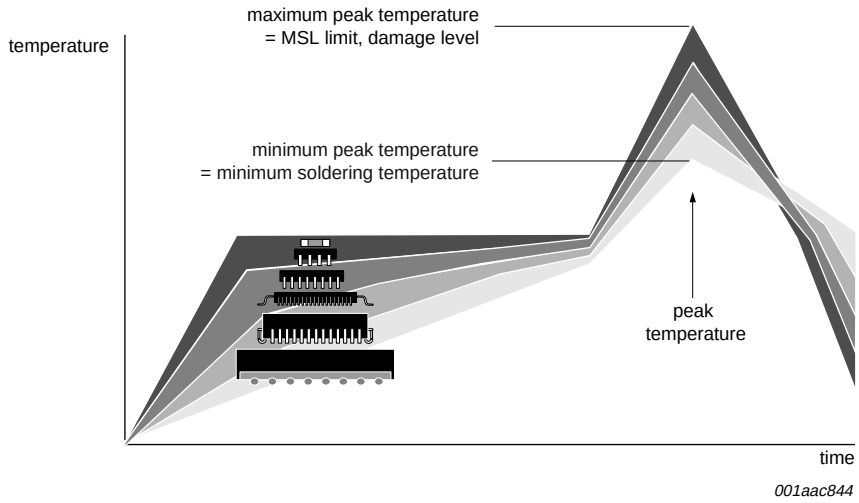
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 36. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 23.



MSL: Moisture Sensitivity Level

Fig 23. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

16.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

16.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in *Application Note AN10365 "Surface mount reflow soldering description"*.

16.3.4 Cleaning

Cleaning can be done after reflow soldering.

17. References

[1] **The I²C-bus specification —** version 2.1, January 2000.

[2] **BS EN 62106 —** Specification of the radio data system (RDS) for VHF/FM sound broadcasting in the frequency range from 87.5 to 108 MHz, 2001.

[3] **Data sheet TEF6892H —** Car radio integrated signal processor, 2003 Oct 21.

[4] **JESD22-C101C —** JEDEC standard for charged-device model ESD test method.

[5] **Data sheet SAA6588 —** RDS/RBDS pre-processor, 2002 Jan 14.

[6] **EN 55020 —** Sound and television broadcast receivers and associated equipment-Immunity characteristics- Limits and methods of measurement, May 2002.

[7] **RDS: The Radio Data System —** Dietmar Kopitz and Bev Marks.

18. Revision history

Table 37. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA5766UK_1	20070322	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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21. Contents

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